SUNY Oswego

Electrical and Computer Engineering Department

ECE492

Keck X-ray Pixel Array Detector (PAD) Amplifier Design

By

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Abstract

The first Keck x-ray pixel array detector (PAD) was developed at Cornell University in the late 2000s. X-ray PADs directly detect x-rays and convert them to a voltage. They are composed of a semiconductor detector layer that is electrically bonded to a CMOS integrated circuit for processing and readout. The Keck detector was developed for use at the Advanced Photon Source (APS) in Chicago. It is a high speed, high flux, burst detector that is capable of taking and storing 8 shots with 153ns between shots. The APS has since improved its beamline technology and now can send pulses of x-rays every 77ns, but the original Keck is not capable of handling these speeds. Hence, a new detector must be created that can operate similarly to the Keck, but faster. Methods to create faster pixel electronics for this new detector that follows in the footsteps of the original Keck detector are presented in this paper.

Acknowledgements

I would first like to thank SUNY Oswego and the ECE department for supporting this capstone project. The classes I took there have contributed to my success on this project, and my Microelectronics and Control Systems notebooks have been on my desk during the entirety of this project. I would specifically like to thank Dr. Marianne Hromalik, for recommending me to the position I have taken at Cornell, and for all the help she has given me during the course of this project. I would also like to thank Dr. Mark Tate for all the help he has given me. He has acted like a second advisor for this project and his knowledge has been invaluable. Dr. Julia Thom-Levy has also giving me much support and has been instrumental to my success at Cornell.

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1 Introduction

1.1 Problem Specification

X-ray detectors are used to conduct experiments on matter. X-rays have wavelengths on the order of Angstroms (Å), making them particularly useful for working at molecular and even atomic scales. These experiments can range from finding the structure of proteins to finding the rotational shift between 2 sheets of atoms. These studies are conducted at x-ray beamlines, often from synchrotron sources. The synchrotron sources can provide a high-flux pulse train of x-rays in tight bunches. A sample can then be place on the beamline, where x-rays will strike it. In these studies, there are often different characteristics that want to be evaluated so specific detectors are designed to best suit the needs of studies.

The Keck PAD is one such detector. It was designed by the Gruner research group at Cornell University in the late 2000s [1]. The Keck PAD is a burst x-ray detector. This means that this detector is designed for taking a collection of images (also called frames), with short times in between frames. Keck 1 and Keck 2 are able to take shots with frame times of 153ns. These images are taken faster than they can be readout to a computer, so they are stored on the pixel. After the shots have all been taken, the data is readout to an FPGA (Field Programable Gate Array). This readout process happens on the order of milliseconds, whereas the actual image capturing is on the order of nanoseconds.

This project is at the request of the Advanced Photon Source (APS). The APS is upgrading their beamline to decrease the time between x-ray pulses. The APS needs a new detector that has a burst speed that can match the speed of their new pulse train.

The Keck PAD is a cutting-edge piece of hardware, so some of the technical specification are still being worked out. While the APS is leaving some design choices up to the engineers designing the detector, many are pre-determined based on the specifications of the beamlines where it is designed to operate. For example, the physical materials that comprise the sensor layer are in great part determined by the energy of the x-rays it will detect. The most unwavering of specifications is the speed. This detector needs to take shots every 77ns. This is the length of time that separates the x-ray pulses, and the detector needs to be able to function at this speed, or it will not be useful. Other specifications are not set in stone, but will align with those of detectors that the group has designed previously. The focus of this project is the amplifier design, but in investigating the amplifier, the whole pixel needed to be investigated broadly. For example, the APS has not specified the amount of power that this design can dissipate when idle, but previous experience in the group has dictated that 100 μW per pixel is acceptable [1]. A full table of tentative specifications is presented in Table 1.

Pixel Size	150 µm × 150 µm
Tile Size	128 × 128 pixels
Idle Power	> 100µW
Sensor	500µm Silicon
Full Well (low gain)	8000 8-keV x-rays
Full Well (high gain)	1200 8-keV
Noise (high gain)	> 1 x-ray
Minimum Frame Time	77ns
Transistor Process	TSMC 180nm 1.8V
Charge Carriers Collected	Holes

Table 1: Design Parameters

Parameter such as the full well capacity, the energy of x-rays, and the sensor material are still being decided, so those of the original Keck have been used as stand-ins. The size of the full well is the only undecided parameter here that has significant impact on the design of pixel electronics. Different sensor materials and the energy of x-rays can all be simulated with simple multipliers on what already exists, but the size of the full well directly correlates to the speed performance of the device. It has currently been chosen to be larger than what may be needed. If it is decided that the full well does not need to be as large, then it can be changed, which should only improve the performance of the detector. The process is also still subject to change. The Keck 1 & Keck 2 are designed on a 250nm 3.3V process, but the more recent PADs created have been on 180nm 1.8V processes. Besides being more modern, smaller processes generally lead to speed increases (at the cost of inherent gain). This would also allow for easy future implementation of

modern features from other PADs into Keck 3, such as adaptive gain coming that was implemented in another successful PAD developed by the Cornell Detector Group and the APS – the MMPAD 2.0 [2].

The circuit being designed is an integrated circuit, meaning that to produce a physical device, it must be fabricated at a foundry. This process is slow and expensive, making it was not feasible to have any physical chips made during this project. Instead, simulation will be used to verify functionality.

This project was conducted by Nicholas Brown while working in the Gruner/Thom-Levy Biophysics research group. This group is a part of the Lab of Atomic and Solid-State Physics at Cornell University. This project was proposed during the Spring 2022 semester. Work began on it in the Summer 2022 semester and the project was completed in the Fall 2022 semester. This project was under the advisement on Dr. Marianne Hromalik from the SUNY Oswego ECE Department.

1.2 Background

1.2.1 Fundamentals of X-ray PAD Design

X-ray PADs are created out of 2 layers. The top layer is the detection layer. This layer is formed out of a semiconductor and serves to convert x-rays into charge. This layer is connected to the ASIC (Application Specific Integrated Circuit) layer via bump bonds. Both the ASIC and sensor layer are pixelated, giving the detector the ability to capture two-dimensional information. Figure 1 is a visual representation of this design.

The ASIC layer is divided into many individual pixels, each of which contains identical circuitry. The design of this circuitry can vary depending on the class of detector. Digital PADs

currently dominate the field, but analog PADs also exist and have their own advantages and disadvantages. These two classes of PADs are explained at in sections 1.2.3 and 1.2.4.

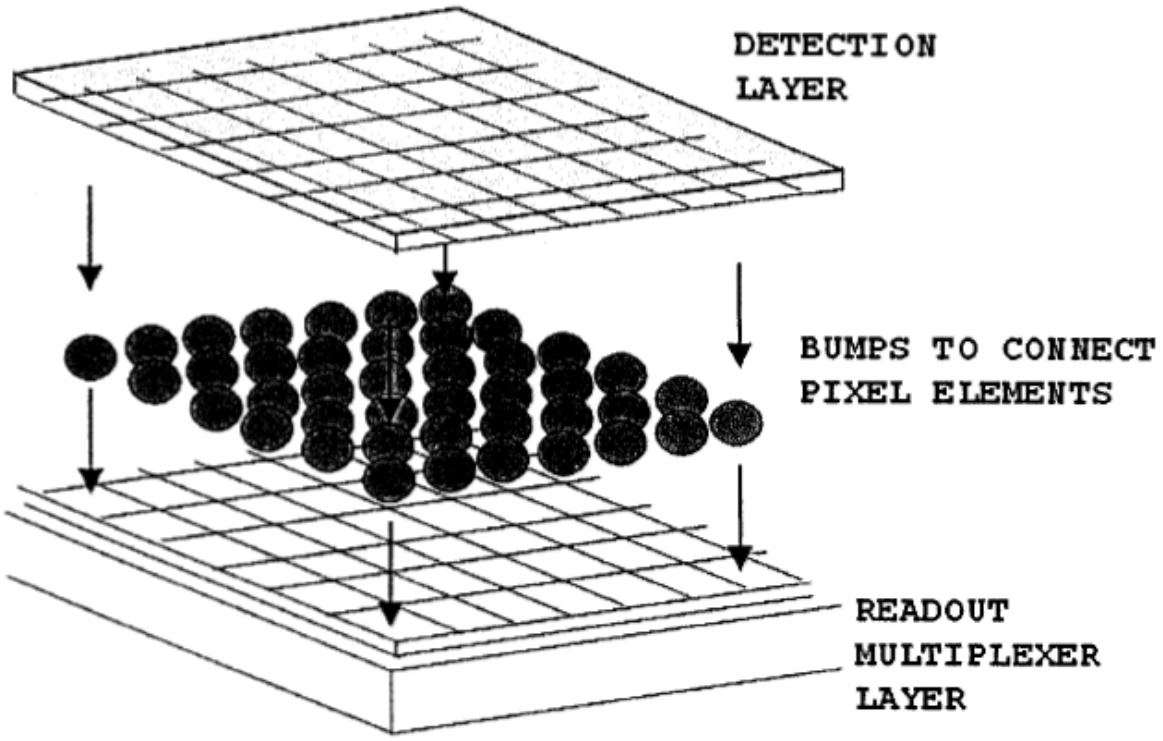

Figure 1: Visual representation of the architecture of a Pixel Array Detector. The top layer is made of a semiconductor such as silicon or cadmium telluride. The bottom layer is a custom designed ASIC for processing and readout of the x-ray signals. The bump bonds connect the layers together. Adapted from **[3]**.

1.2.2 X-ray Detection in Semiconductors

Direct x-ray conversion using semiconductors has become the predominant collection method in recent years. Before semiconductor detection was used, charge coupled devices (CCDs) were used. These devices were an indirect way of capturing x-rays, but have hit a limit of further development, sparking interest pixel array detectors instead (PADs) [4].

These PADs collect x-rays via a semiconductor detection layer. Silicon is a popular semiconductor material for detection layers but others such as cadmium telluride (CdTe) exist. The materials that comprise the detection layer have significant impact on the energies in which the detector can operate. While silicon is popular, it is not good at collecting high energy x-rays as seen in Figure 2. Other semiconductors are of interest due to their different properties. Cadmium telluride is one such material. Figure 2 shows that cadmium telluride is significantly better at collecting high energies x-rays than silicon [5].

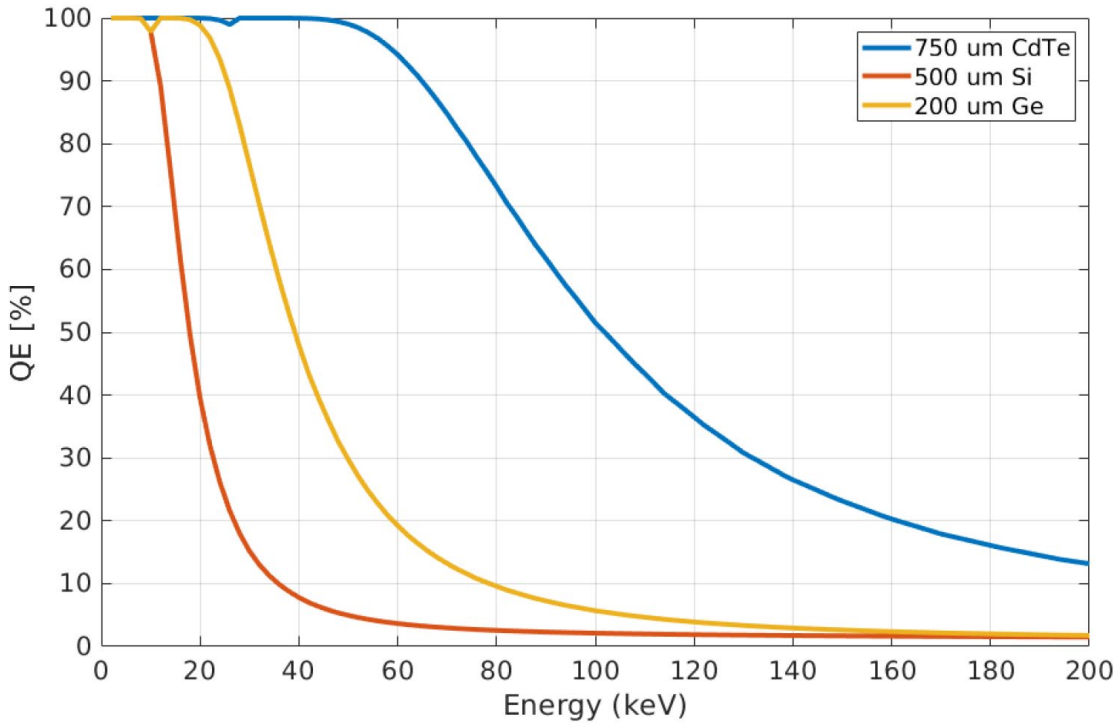

Figure 2: Collection efficiency 750µm cadmium telluride, 500µm silicon, and 200µm germanium. Adapted from **[5]**.

When a photon strikes a semiconductor layer, it is converted into electron-hole pairs [1]. These electron-hole pairs can then be separated by a large voltage bias that is applied over the

detection layer. Depending on the polarity of this detector bias, either the holes or the electrons are collected into the ASIC layer. The operating principle for holes and electrons is similar, with some detector being able to collect both.

The number of electron-hole pairs is dependent on the energy of the x-rays and the detection layer material. The amount of electron-hole pairs, $N_{eh,}$ is defined by $N_{eh} = E_{ph}/E_{pair}$ where E_{ph} is the photon energy and E_{pair} is the electron-hole pair creation energy for the material. In silicon E_{pair} is approximately 3.65 eV [1]. This relationship is important in determining how much charge the ASIC needs be able to process. For example, at a full well of 8000 8 keV x-rays will produce 2.816pC of charge in silicon and the detector needs to be designed to handle this amount of charge. In the interest of speed and area, the detector should be designed to accommodate a full well of charge, but not any more.

1.2.3 Digital X-ray Detectors

Digital x-ray detectors are often called photon counting detectors because digital detectors count photons discretely as packets of charge. This means that they have very low noise and are resistant to the low levels of dark current present in the detection layer [1]. These PADs still consist of a semiconductor and ASIC layer. The semiconductor layer acts the same as in an analog detector, the differences lie in the electronics within the ASIC layer.

Digital detectors are primarily composed of three parts, an analog stage to limit the bandwidth and amplify the signal coming from the detector layer, a discriminator that determines when the signal reaches a specific threshold, and a counter that counts the amount of times that the discriminator reaches the threshold [6]. Figure 3 shows a block diagram of these detectors. This counting action is relatively slow and these detectors can only handle about 10 million x-

rays per pixel per second [1]. This means that a photon counting detector can only count 1 x-ray every 100ns, making this architecture impossible to use in the update Keck design.

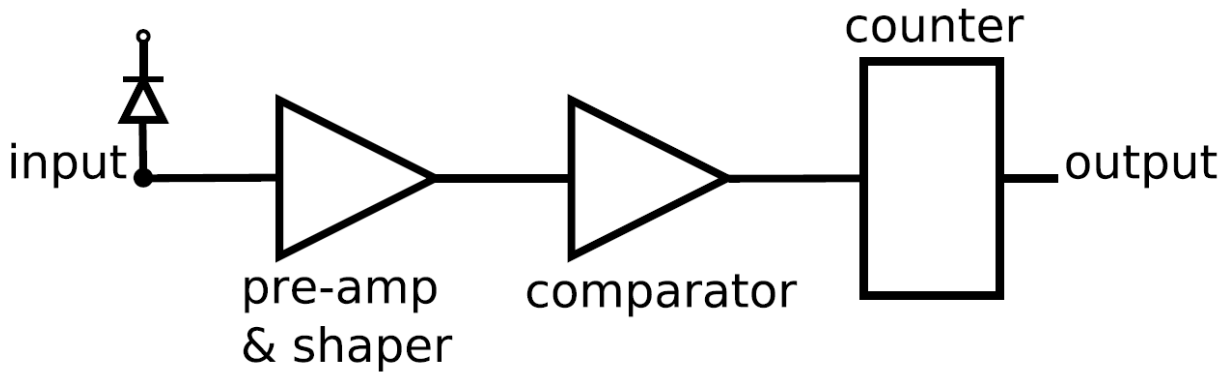

Figure 3: Block diagram of a digital x-ray detector. Adapted from **[1]**.

1.2.4 Analog X-ray Detectors

Analog x-ray detectors (also called integrating detectors) are the primary focus of this research. These detectors are able to process much more charge than their digital counterparts, handling fluxes of nearly 10^{12} photons per pixel per second [1]. This means that an analog detector can process thousands of photons per nanosecond, making them the only possible architecture for ultra-fast speeds.

This class of detectors are again formed by an ASIC layer and a detection layer. The ASIC layer is made from two stages; the front-end, and the sampling/storage stage. Analog detectors integrate the charge created by x-rays onto a front-end capacitor (C_F). This converts the charge into a proportional voltage following $V = Q_{IN}/C_F$. The resulting voltage is then either read off the ASIC to an FPGA (Field Programable Gate Array), or it is held on the chip in the storage stage and read off later. The front-end capacitor is then reset via a switch that shorts both terminals of the device together. A simple analog detector is presented in Figure 4.

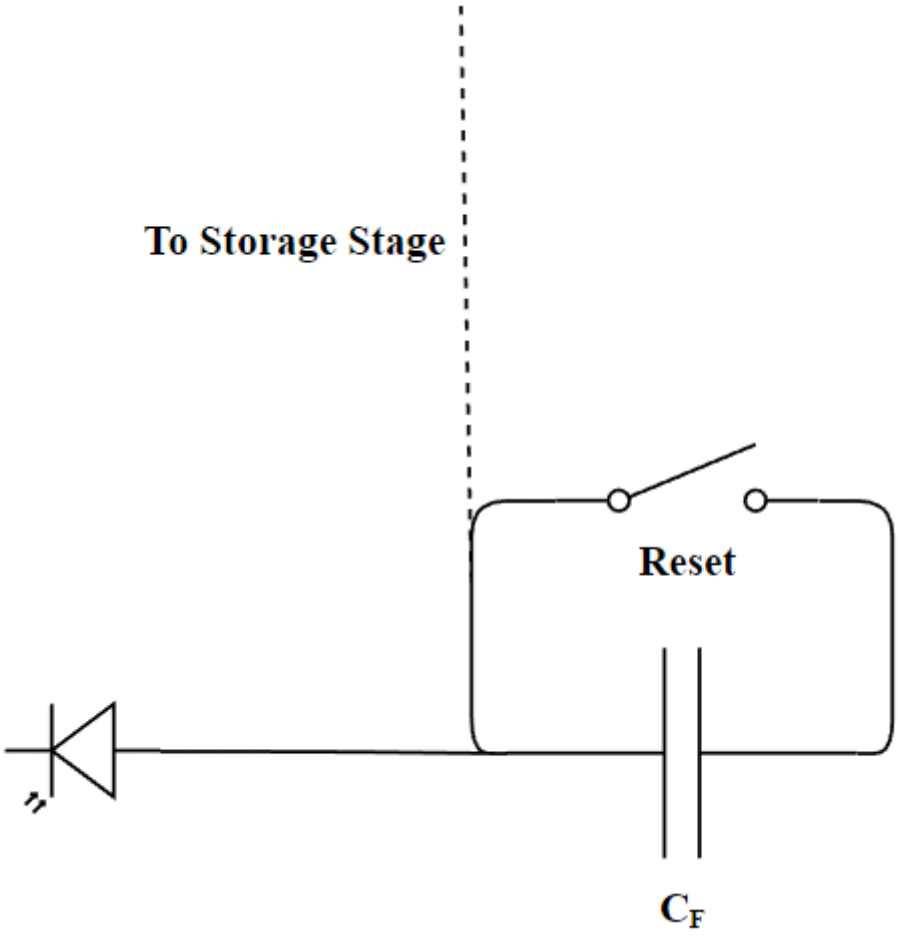

Figure 4: Simple front-end architecture utilizing a single integration capacitor and a reset switch

Because the Keck PAD operates at very high speeds, it is not able to read off data in real time. To store voltages on the chip, banks of switched capacitors are included in the storage stage. These capacitors are switched in at the beginning of a shot, and switched out at the end of a shot. These capacitors then hold the voltage from the front end, and as long as the leakage current of the switches is low, they will hold this voltage for a relatively long time. This means that after all the shots have been taken, the values can then be read out shot by shot, pixel by pixel.

2 Pixel Electronics

2.1 SPICE

Integrated circuits utilizing MOSFETs are generally complicated designs that are hard to represent using hand calculated mathematical models. Modern MOSFETs have hundreds of different metrics that can affect performance. This means that any model done by hand will either be too complex to handle, or not as accurate as it could be, leading to potential unexplained behaviors. This makes it difficult to verify the functionality of a design.

A designer may turn to physically creating the circuit on a breadboard and verify functionality that way. This works in general analog circuits, but this cannot be applied to ASICs. Integrated circuits are intended to be fabricated at a foundry. They are designed on a specific process that the foundry provides with hundreds of different performance characteristics for devices. The chips that foundries produce use small components, with transistors on the scale of nanometers. Discrete components do not provide the same level of accuracy that is required. One of the most crucial aspects of circuit elements that designers can change is their size. Discrete transistors have a fixed size. For transistors the width and length both have significant impact on the performance of the device. The ratio of width and length is main performance parameter that designers care about, but the absolute values have immense impacts on the high-speed performance of the device. All of this combined means that a designer can't just build a circuit out of discrete parts to verify functionality, so instead they turn to simulations.

SPICE (Simulation Program with Integrated Circuit Emphasis) is a simulation language with an emphasis on integrated circuits [7]. Originally developed in the 1970s, it still is used as one of the leading circuit simulators today. This language allows for DC analysis, AC analysis,

transient analysis, noise analysis, and much more. This language is particularly good a simulating MOSFETs and libraries can be used that allow for the simulation of a foundries specific processes. This language is key in understanding and verifying the functionality of integrated circuits.

SPICE allows for the creation of models of real circuit components such as resistors, capacitors, switches, and MOSFETs. These models follow mathematical equations to describe behavior, but all of this is done via SPICE. Models can be made to follow the behavior of ideal devices, or they can be designed to simulate a realistic device with all its nonidealities. These components can then be connected via nodes to form full circuits. Simulations can then be performed on these circuits to gain insight on the true functionality of the design. This allows for accurate calculations, using all parameters of devices while not overwhelming the designer. It also allows for easy, on the fly changes to the circuit, letting the designer experiment with their circuit.

This language is used by Tanner, a software suite from Siemens. It is specifically used by T-SPICE and Waveform Viewer, allowing for simulation and plotting of output results when applicable. Circuits can be designed by hand, using SPICE commands, or they can be designed using S-Edit, a visual GUI that allows for users to place and connect components in a very visual way. While the schematic view that S-Edit provides is useful, simply making circuits in SPICE was used more frequently in this research. Tanner and by extension, SPICE, is heavily used in this project. All of the results presented here do no take the physical layout of the device into consideration. Parasitic elements manifest themselves when laying out a circuit, but they are out of the scope of this project.

Figure 5 shows an example circuit designed using SPICE. Line 21 indicates that this device is a subcircuit. This makes the device easily callable by other files as a “black box” with

pins; ISS_AB, Vinn, Vinp, Vout, Gnd, and Vdd. This makes it simple to place this device into different test bench files, where only simulation commands exist. One file can exist to solely investigate transient performance, while another can exist to test its AC characteristics. It can also allow for the device to be easily repeated if desired.

Lines that begin with "." are generally reserved for simulation commands. If the first term in a line begins without a ".", it is the declaration of the name of a component. The first letter of this name dictates which component it is. For example, lines 23 and 24 of Figure 5 declare ideal resistors because they begin with "R". These devices have 2 terminals. Resistor RR1 has its terminals tied to nodes "N_7" and "N_6", with a resistance value of "R_LCMFB", which is a parameter. Components that begin with "M" are MOSFETs. These devices are 4 terminal devices that have connections to drain, gate, source, and bulk (from left to right). This specific file use nonideal MOSFETs, which follow the model "nch" and "pch". These models are provided by a library file and follow the specification of TSMC's 180nm 1.8V process.

```
.subckt ClassABResistors ISS_AB Vinn Vinp Vout Gnd Vdd

RR1 N_7 N_6 R_LCMFB
RR2 N_8 N_7 R_LCMFB
MM7 N_8 N_7 Gnd Gnd nch W=600n L=180n AS=540f PS=3u AD=540f PD=3u
MM8 Vout N_8 Gnd Gnd nch W=1.2u L=180n AS=1.08p PS=4.2u AD=1.08p PD=4.2u
MM6 N_6 N_7 Gnd Gnd nch W=600n L=180n AS=540f PS=3u AD=540f PD=3u
MM5 N_2 N_6 Gnd Gnd nch W=1.2u L=180n AS=1.08p PS=4.2u AD=1.08p PD=4.2u
MM0B N_4 ISS_AB Gnd Gnd nch W=360n L=180n AS=324f PS=2.52u AD=324f PD=2.52u
MM0A N_3 ISS_AB Gnd Gnd nch W=360n L=180n AS=324f PS=2.52u AD=324f PD=2.52u
MM1 N_6 Vinn N_5 Vdd pch W=1.2u L=180n AS=1.08p PS=4.2u AD=1.08p PD=4.2u
MM2 N_8 Vinp N_1 Vdd pch W=1.2u L=180n AS=1.08p PS=4.2u AD=1.08p PD=4.2u
MM1A N_3 Vinn N_1 Vdd pch W=1.2u L=180n AS=1.08p PS=4.2u AD=1.08p PD=4.2u
MM1B N_4 Vinp N_5 Vdd pch W=1.2u L=180n AS=1.08p PS=4.2u AD=1.08p PD=4.2u
MM2A N_1 N_3 Vdd Vdd pch W=1.8u L=180n AS=1.62p PS=5.4u AD=1.62p PD=5.4u
MM2B N_5 N_4 Vdd Vdd pch W=1.8u L=180n AS=1.62p PS=5.4u AD=1.62p PD=5.4u
MM3 N_2 N_2 Vdd Vdd pch W=1.2u L=180n AS=1.08p PS=4.2u AD=1.08p PD=4.2u
MM4 Vout N_2 Vdd Vdd pch W=1.2u L=180n AS=1.08p PS=4.2u AD=1.08p PD=4.2u
MM3A Vdd N_3 Vdd Vdd pch W=1.8u L=180n AS=1.62p PS=5.4u AD=1.62p PD=5.4u
MM3B Vdd N_4 Vdd Vdd pch W=1.8u L=180n AS=1.62p PS=5.4u AD=1.62p PD=5.4u
.ends
```

Figure 5: An example of a SPICE circuit. This design is an early iteration of the Class AB amplifier used for this project.

Simulation in SPICE required the creation of numerous test benches. Components are created individually as subcircuits These testbenches are used like a hub, to collect devices at a black box level and connect them. Simple devices such as capacitors are created in the testbench. This component level simulation allows for simple implementation of complex device. Instead of needing to repeat and rename the transistors included in a switch, many switches could be created from a single SPICE file. It also allows for these SPICE files to be included in other testbenches.

Parameter are another important tool in the SPICE language. Parameters are similar to variables in more well know language like C or Python allowing for a name to be assigned to a

number. Anytime this name is seen in compilation, it is replaced with the number that it is assigned to. These commands are indicated with ".param" at the beginning of a line. Parameters can also be used in conjunction with other parameters, allowing equations to be calculated. Figure 6 shows a SPICE file where parameters that are set by the user are used to calculated other parameters. Specifically, the parameter "xrays" can be set by the user, and the "charge" parameter is then calculated from this value.

Parameters allows for simplification and flexibility to be built into SPICE files. Firstly, values can be calculated using parameters. These values can then be repeated multiple times in SPICE files. This also allows for a great level of flexibility. Parameterization of all numerical characteristics allow for changes to be done on the fly. The ability to calculate based off of parameters gives one value change the ability to ripple through a testbench, changing dozens of other parameters. Parameters can be passed between files in SPICE, so a single parameters file can be created that allows for all parameters to be imported into a testbench. This allows for parity between multiple testbenches.

```
* Input pulse stuff

.param xrays = 2000                          * Set amount of x-rays for either input
.param pulseDur1 = "10n"                     * Sets duration for 4 piece input (based on Julians Beckers work)
.param pulseDur2 = "7n"                      * Sets duration for 3 piece input (based on Divya Gadkari work)

* Dont touch these unless you know what you are doing
.param tau = "(iPulseTime1/15)*shotMul"
.param iPulseTime1 = "pulseDur1*shotMul"                    * Don't touch
.param iPulseTime2 = "pulseDur2*shotMul"                    * Don't touch
.param charge = "xrays*.352f"                       * Amount of charge to be collected, full well is 4693fF or ~2816fC
.param iCharge1 = "-(charge/iPulseTime1)"          * Charge is sent in a pulseTime pulse, this finds the equivalent current
.param iCharge2 = "-(charge/iPulseTime2)"
.param iDelayTime = B                        * Sets when the pulse will start, should be at the begining of window B (shot time)
.param randomness = 2
```

Figure 6: An example of parameters in SPICE.

2.2 Pixel Architecture

As stated in section 1.2.4, the pixel ASIC can be evaluated in two parts; the front-end and the sampling/storage stage. The front-end is most related to the speed of the device, making it the most important part of this design. The sampling stage is relatively slow and not read out as shots are taken, meaning it has less bearing on the speed of the device. The capacitor bank that is used to store the frames has been modeled and investigated, but the readout process has not.

The front-end is the focus of this project. Speed is of the upmost importance for this device. This detector needs to be able to take frames every 77ns at the very least. This specification is unwavering and is the center of this project. Multiple architectures have been investigated, and different designs within these architectures have been considered.

Since this detector is an analog detector, it follows the principles presented in 1.2.4. The device will have a capacitor that will accumulate charge that is created by the incident x-rays. This pixel will have a total of 77ns in which it must reset, clearing any residual charge off of integration capacitors and storage capacitors, integrate, collecting charge and producing a proportional voltage output, and switch, disconnecting the current capacitor and connecting the next storage capacitors. The pixel will do this for all eight shots.

The guiding principles of an architecture are quite simple. From a black box perspective, a device needs to be designed that can receive incoming charge, and return a proportional voltage to the storage stage. This is represented in Figure 7. This input stage needs to be able to hold the pixel electrode at a stable voltage bias, to prevent capacitive cross-talk between pixels [3]. It also needs to be able to compensate for the parasitic input capacitance that will form at the input due

to the detector layer, amplifier input devices, and the bump bonds [1]. It again needs to be able to meet the requisite speeds while doing this.

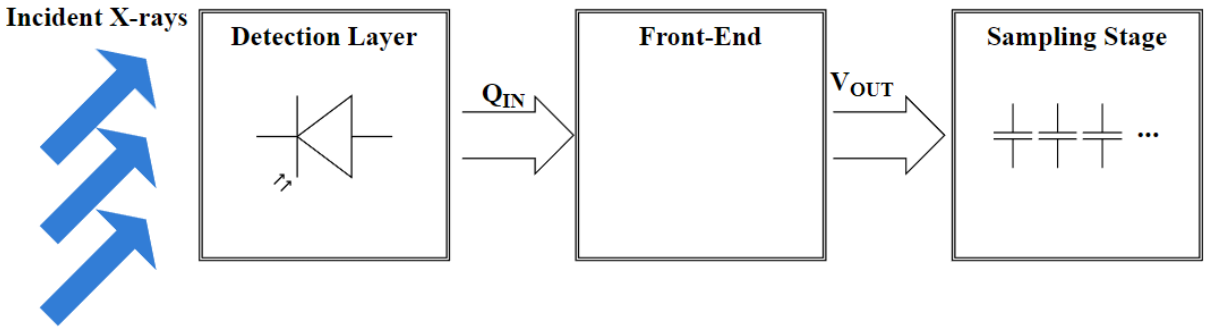

Figure 7: Block diagram of a single pixel in the Keck PAD.

2.2.1 Source Follower Per Detector Input Stage

The Source Follower per Detector (SFD) is one of the simplest input architectures. This architecture uses only a capacitor and a reset switch. One of its biggest strengths is it simplicity. This design is easy to implement, and utilizes only a single transistor for a reset switch. The only voltages required would be V_{DD} and ground. This device is also very power efficient because the transistor is just used as a reset mechanism. This means that at idle, the circuit should draw no power. Even during slewing situations, the device would not consume power. Only during resets would any power be drawn. This means that a device based on this architecture can have excellent thermal performance. This device follows $V = Q_{IN}/C_F$. The voltage at the pixel electrode changes to a voltage proportional to the charge, and this voltage depends on the size of the feedback capacitor (C_F). This design has been used in focal plane detectors in the past, but it has largely been avoided in PADs due to its myriad of issues [3].

The first issue that this architecture has is its inability to hold the pixel electrode at a steady bias. The voltage at the back end of the capacitor is tied to ground meaning that the voltage on the pixel electrode must change. This changing voltage means that pixels are vulnerable to capacitive cross-talk.

Capacitive cross-talk arises from the layout of the device. Recall a simple capacitor is constructed from two plates of metal, separated by a dielectric. The pixel array nature of this device means that all pixels see adjacent pixels and their electrodes and form capacitors with one another. If one pixel receives very high signal on its input, a large voltage change will follow. This change in voltage will cause currents in the adjacent pixels following $I = C * \frac{dV}{dt}$. This current will then be processed by those pixels as incoming charge, resulting in more counts than what actually occurred. This leads to blurry images and is not desirable.

The second issue that this architecture faces is its weakness to parasitic capacitance on the input. Shown in Figure 8, C_{IN} is the parasitic capacitance and can be on the order of hundreds of femtofarads. Incoming charge will be divided over these two capacitances, following the equation shown in Figure 9. Considering that the integration capacitor is generally anywhere from tens of femtofarads to a few picofarads this parasitic capacitance is not just significant, it can be even be dominant. This can be mitigated by using a very large C_F, but that requires a significant amount of area, and also makes reset speeds much slower. Changing the size of C_F also doesn't fully remedy the issue, just makes it less noticeable. Even if C_F was one hundred times larger than the C_{IN}, the charge collection efficiency (CCE) would still only be around 99%.

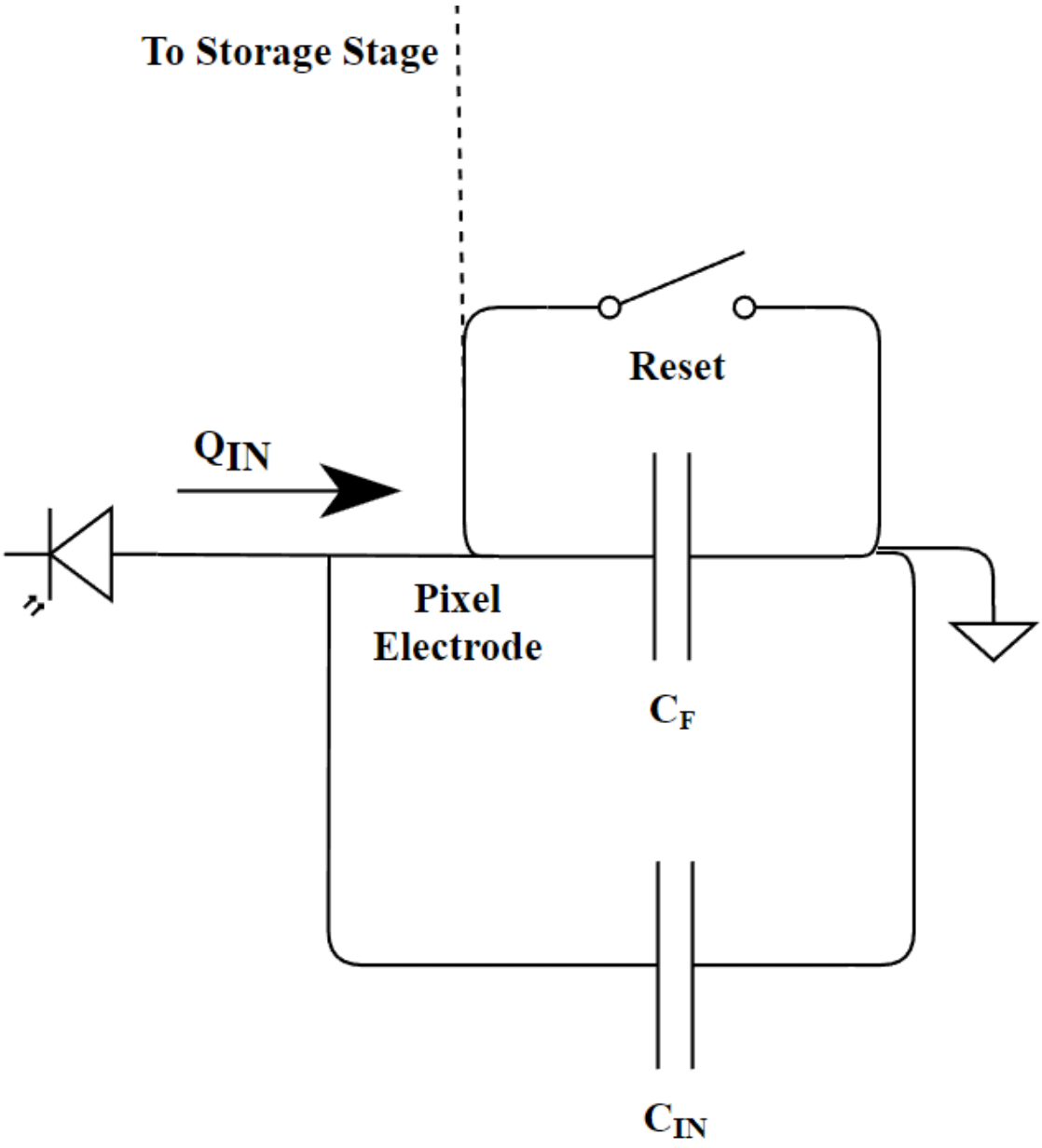

Figure 8: Source Follower per Detector (SFD) input stage with a parasitic input capacitance C_{IN}.

$$CCE = \frac{C_F}{C_F + C_{IN}}$$

Figure 9: Charge collection efficiency (CCE) of an SFD.

2.2.2 Capacitive Transimpedance Amplifier

An alternative to the SFD is the capacitive transimpedance amplifier (CTIA) shown in Figure 10. This architecture utilizes an operational amplifier to put the integration capacitor (C_F) in negative feedback. This design also shows C_L to represent a storage capacitor and C_{IN} to represent the lumped parasitic input capacitance. This input capacitance will be slightly larger, due to the capacitance coming from the input of the amplifier, which will be discussed in more detail later. This device is considerably more complicated than the SFD, but it comes with significantly improved characteristics.

This architecture is able to hold the pixel electrode at a steady voltage. Since this circuit utilizes and operational amplifier, assumptions can be made. Firstly, the amplifier has infinite input impedance meaning no current can flow into the input of the amplifier. Secondly, amplifiers have very large DC gain, A, which can be on the order of 10^5 or 10^6. Lastly, the amplifier will form a "virtual short circuit" between the two inputs. This means that the if the non-inverting input is tied to some reference voltage V_{REF}, then the amplifier will try to keep the inverting input at V_{REF} as well. In practice, this means that as input charge enters the system, the amplifier will change the voltage at the output of the amp (V_{OUT}), not at the pixel electrode. This will prevent the capacitive cross talk that existed in the SFD.

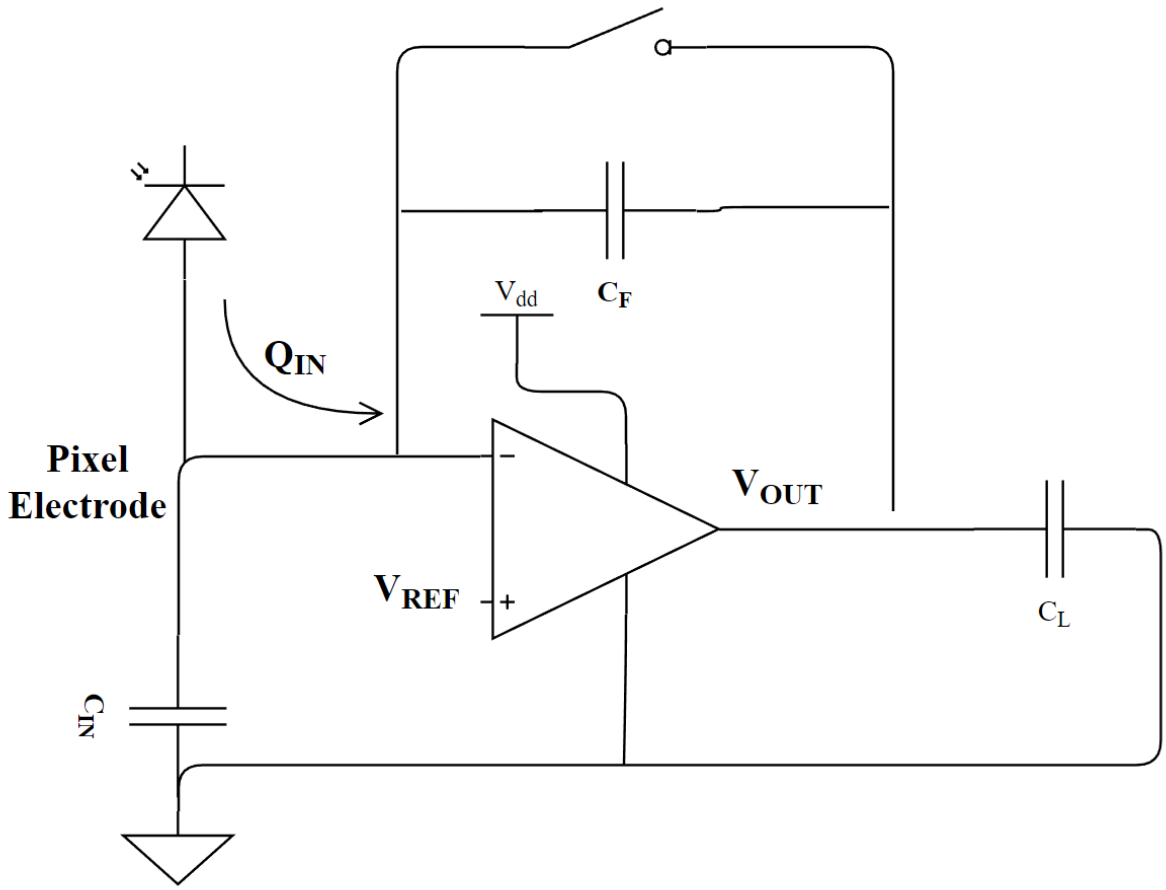

Figure 10: A simplified schematic of the CTIA architecture with feedback capacitance of C_F, parasitic input capacitance of C_{IN}, and a load capacitor of C_L to act as analog memory. A reset switch is shown at the top.

This architecture is also much better at dealing with the effects of the parasitic input capacitance. In the SFD, the best way to deal with a large parasitic capacitance was to make C_F very large. Whereas before the charge collection efficiency saw just a charge division over C_F and C_{IN}, this device will now see a Miller multiplication of C_F on the input node and C_{IN}.

Millers theorem states that an impedance, Z, that is connected between two non-grounded nodes, X and Y, in a linear circuit can be broken up into two impedances Z_1 and Z_2. These two

impedances are connected to one of the original nodes and ground [8]. This can be seen in Figure 11. The current flowing through Z from node X to node Y must be equal to $(V_X - V_Y)/Z$. So, for the two circuits in Figure 11 to be equivalent, the same current must flow through Z_1. Meaning,

$$\frac{V_X - V_Y}{Z} = \frac{V_X}{Z_1}$$

When solved for Z_1,

$$Z_1 = \frac{Z}{1 - \frac{V_Y}{V_X}}$$

The same can be applied to Z_2 yielding,

$$Z_2 = \frac{Z}{1 - \frac{V_X}{V_Y}}$$

When Miller effect is applied to a capacitor, which has an impedance of $\frac{1}{sC}$,

$$Z_1 = \frac{\frac{1}{sC}}{1 - \frac{V_Y}{V_X}}$$

$$Z_1 = \frac{1}{s(C * \left(1 - \frac{V_Y}{V_X}\right))}$$

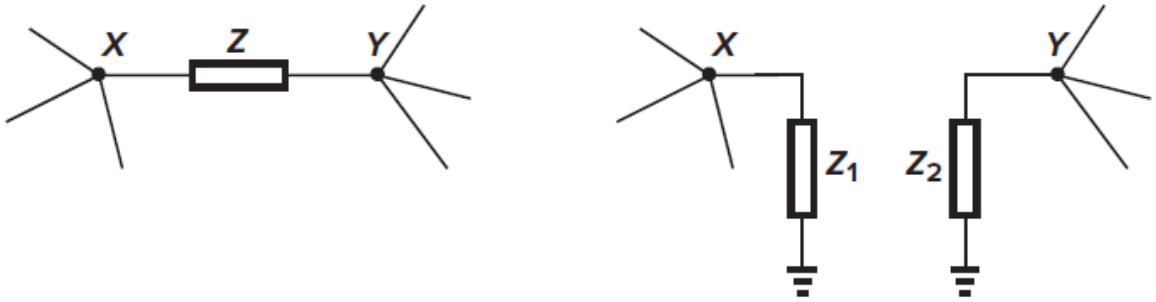

Figure 11: Visualization of a circuit where Millers theorem can be applied. Adapted from **[8]**.

This equation for Z_1 shows that the capacitance at the node X side is multiplied by $\left(1 - \frac{V_Y}{V_X}\right)$. This idea can be applied to C_F in the CTIA architecture. This capacitor is placed between nodes V_{inn} and V_{out}. By using Millers theorem, it can then be broken up into two equivalent capacitors, C_{F1} and C_{F2}. The capacitor on the input side will then have an equivalent capacitance of $C_F * \left(1 - \frac{V_{out}}{V_{inn}}\right)$ but, $\frac{V_{out}}{V_{inn}}$ in this circuit is simply the gain of the amplifier, -A. Perhaps a more concise way of representing C_{F1} is therefore $C_F * (1 + A)$. This means that the value of C_F at the input is significantly greater, without increasing the actual size of C_F. Its new charge collection efficiency is shown in Figure 12. As stated above, and amplifier should have very large gain meaning that for all reasonably sized C_F, $C_F * (1 + A) \gg C_{IN}$. This assumption means that the device will collect 100% of the charge, thereby completely mitigating the impact of the input parasitic capacitance.

$$CCE = \frac{C_F * (1 + A)}{C_F * (1 + A) + C_{IN}}$$

Figure 12: Charge collection efficiency of the CTIA architecture.

While the CTIA is complex, area hungry, and power hungry, its ability to prevent pixel-to-pixel capacitive cross talk, and its resistance to parasitic input capacitance makes is a clear-cut

winner over the SFD. The CTIA is the architecture used in the original Keck, and it will continue being used in the design of Keck 3. Figure 13 shows a simplified schematic of the entire pixel circuitry of the Keck 1. The CTIA can be seen in the front-end, where the C_F capacitors act as feedback capacitors and the C_S capacitors act as storage devices. Parasitic input capacitance is not shown.

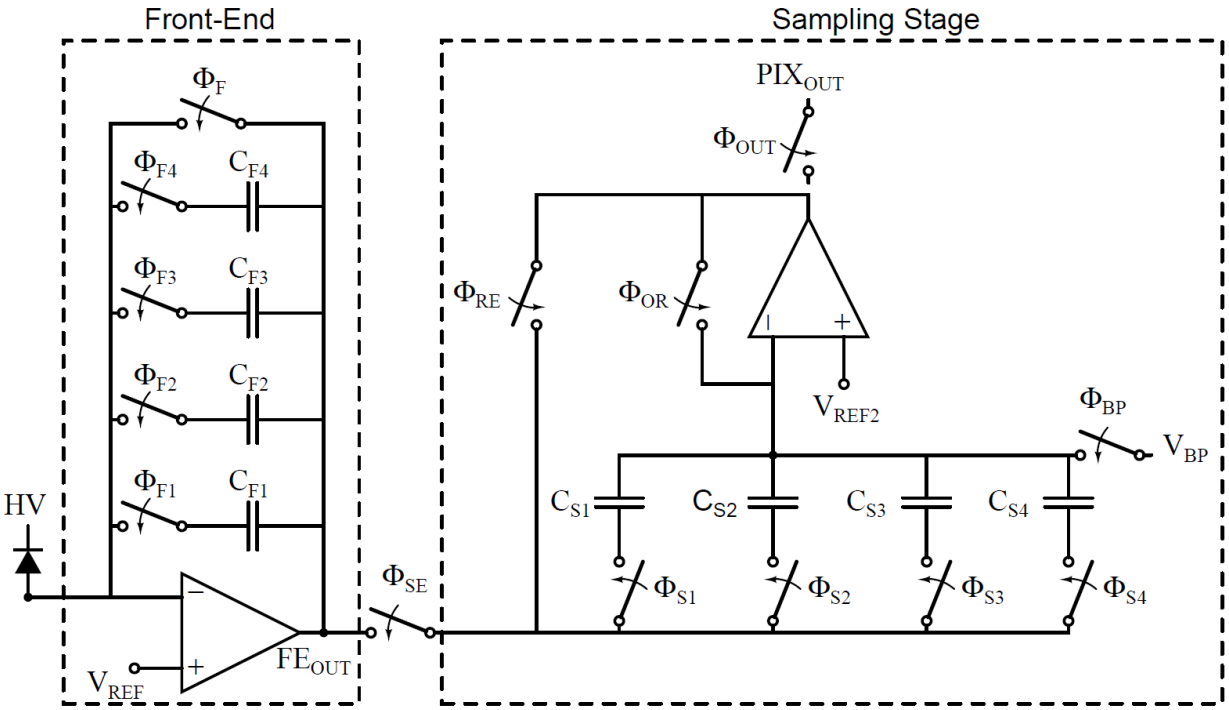

Figure 13: Simplifier drawing of the pixel circuitry in the original Keck PAD. This was used as an outline to guide the design of new pixel circuitry. Adapted from **[1]**.

2.3 Amplifier Design

2.3.1 Introduction

The most important piece to this design is the operational amplifier. This device needs to be fast, power efficient, have high gain, have high slew rate, and be simple as to minimize bias

routing and area. It is also desirable to make this device on the 180nm technology to allow for easy implementation of features from other PADs, such as adaptive gain [2].

A visualization of the final design can be seen in Figure 14. This design can be broken into three different pieces that have their own function. These pieces are the flipped voltage followers (I_B (M_{0A}), M_{1A}, M_{2A}, and I_B (M_{0B}), M_{1B}, M_{2B}), the differential amplifier with common mode feedback (M_1, M_2, M_6, M_7) and the differential amplifier with active load (M_5, M_8, M_3, M_4). They form a Class AB amplifier when combined. Their functionalities will be investigated individually for clarity, and then the design as a whole will be discussed.

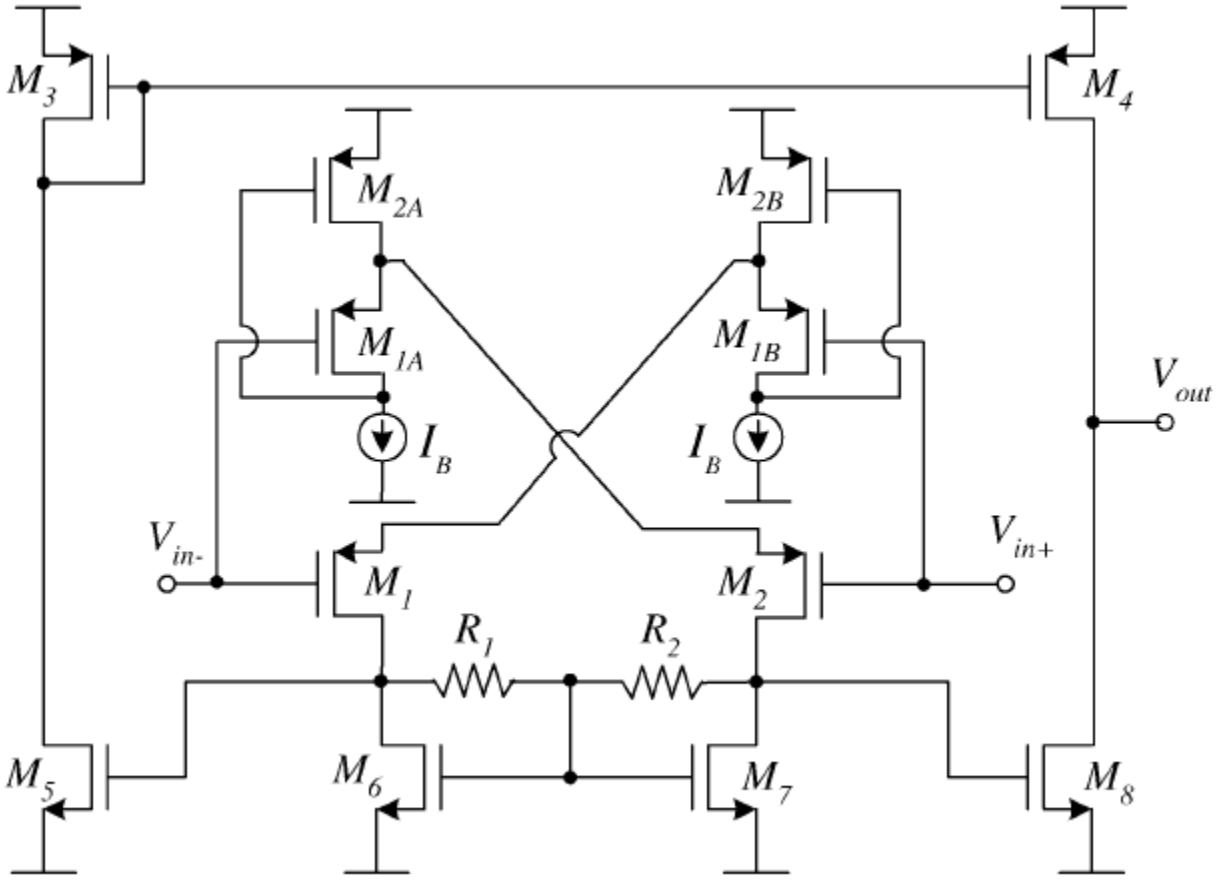

Figure 14: Class AB amplifier with flipped voltage followers (FVFs) for adaptive biases and a resistive bridge for local common-mode feedback (LCMFB). Adapted from **[9]**.

2.3.2 Flipped Voltage Followers

The flipped voltage followers (FVFs) are a simple but essential piece of the amplifiers design. The amplifier uses two FVFs, one for each of the signal inputs in the amplifier. They are constructed from transistors I_B (M_{0A}), M_{1A}, M_{2A}, and I_B (M_{0B}), M_{1B}, M_{2B} in the amplifier design and can be seen in Figure 14. An isolated FVF is shown in Figure 15. The final design uses NMOS transistors in place of the ideal current sources I_B, hence their naming scheme following that of the other transistors. The FVFs are the adaptive bias for the amplifier, that allow it to consume little power when idle, while still allowing for good large signal performance.

The flipped voltage followers act similarly to source followers, but with some differences. The goal of the device is for the output to follow the input, producing a good copy at the output. Since these devices are used as an adaptive current bias, it must also have a low output impedance to source the requisite current [10].

The FVFs act similarly to a source follower. Both circuits have a gain close to one, meaning that they produce a copy of the input at the output node. The flipped voltage follower also shifts the DC level of the input signal at the output. The DC level at the output is determined by $\sqrt{\frac{2I_B}{\beta_1}} + V_{in} + V_{THP}$ [10]. This equation is dependent on the bias current I_B, the M_1 beta parameter β_1, the input voltage V_{in}, and the threshold voltage of the PMOS V_{THP}. This DC level shift is important when this device is connected to the next stage, the differential amplifier with common mode feedback.

Another important property of the FVFs is their ability to source current. These devices must be able to source more than the bias current, so they can act as an adaptive bias circuit. This means that the FVFs must have a low output impedance. The output impedance is estimated to

be about 20Ω-100Ω [10]. It can be found more rigorously using $\frac{1}{g_{m1A}*g_{m2A}*r_{o1A}}$ where g_{m1A} is the transconductance of transistor M_{1A}, g_{m2A} is the transconductance of transistor M_{2A}, and r_{o1A} is the output resistance of transistor M_{1A}.

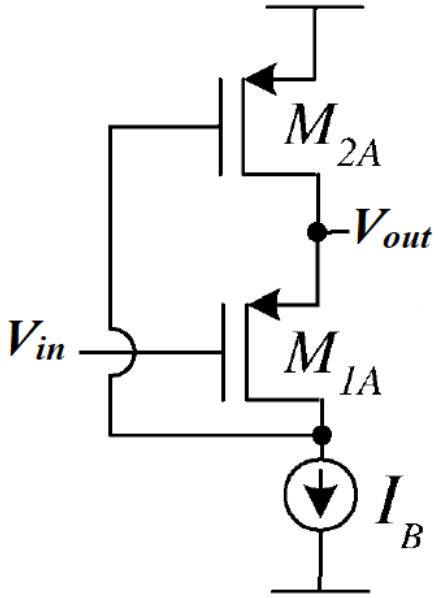

Figure 15: Flipped voltage follower. Adapted from **[10]**.

2.3.3 Differential Amplifier with Common Mode Feedback

The differential amplifier with common mode feedback acts as a gain stages in this device. The input stage is a NMOS differential pair, formed by transistors M_1 and M_2 in Figure 16. The load is contrived from resistors R_1 and R_2, and MOSFETs M_3 and M_4. This load utilizes common mode feedback to create an AC ground at node N [8]. This AC ground means that for differential input signals, the gate voltage of M_3 and M_4 stays constant. This means that this amplifier act like a differential amplifier, but the load biases itself.

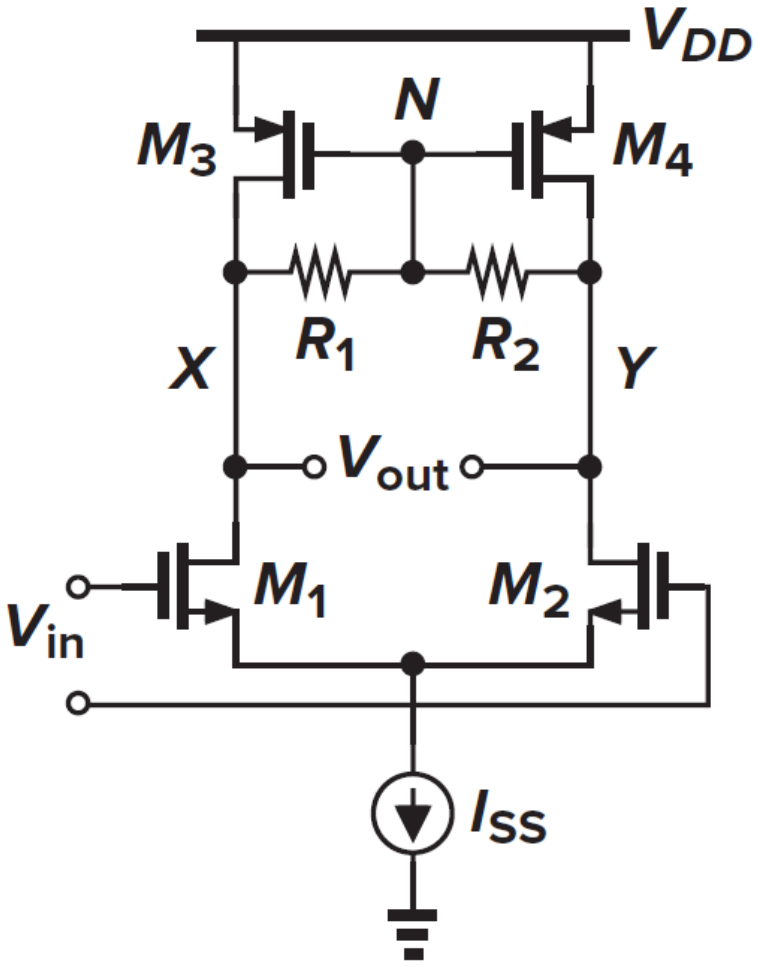

Figure 16: Schematic of a differential pair with common mode feedback. Adapted from **[8]**.

2.3.4 Differential Amplifier with Active Load

The differential amplifier with active load has two inputs and a single output. This can be seen in Figure 17. This amplifier acts as a second stage of amplification, and also makes the output single ended.

The amplifier in Figure 17 has two signal paths. These paths both work together to change the voltage at the output of the amplifier. The first signal path is constructed by M_1, M_3,

and M_4 in Figure 17. Transistor M_3 and M_4 form a PMOS current mirror, meaning that the current flowing in M_3 set the current flowing in M_4 [8]. The drain current flowing through M_3 is the same as the drain current flowing through M_1 because that is the only path that the current can take. Due to the current mirror, any current in M_3/M_1 will be mirrored, and will set the drain current of M_4. If the dimensions of M_3 and M_4 are the same then the drain currents can be defined as $I_{D1} = I_{D3} = I_{D4}$. Assuming all transistors are in saturation, a small voltage increase in the gate voltage of transistor M_1 will lead to an increase in the current drawn by this transistor. This will cause a slight increase in voltage, which will then be mirrored to V_{OUT} by the current mirror.

The second signal path is formed by a single transistor, M_2 in Figure 17. This signal path is much simpler than the first. The MOSFET acts like a common source stage. This stage is inverting meaning that when a small negative voltage is sensed at the gate of M_2, the voltage at the drain would increase.

In the case of a small differential signal, where one input has a small increase in the voltage and the other has a small decrease in voltage, then both signal paths would yield an increase at the V_{OUT} node. This idea also holds if the inputs are flipped, but instead of a voltage increase at the output node. The voltage would decrease. This amplifier has a gain of $g_{mN}(r_{oN}//r_{oP})$, which tends to be below 10 in modern processes [8]. This is relatively low, but the gain of the overall system is supplemented by the differential amplifier with common mode feedback.

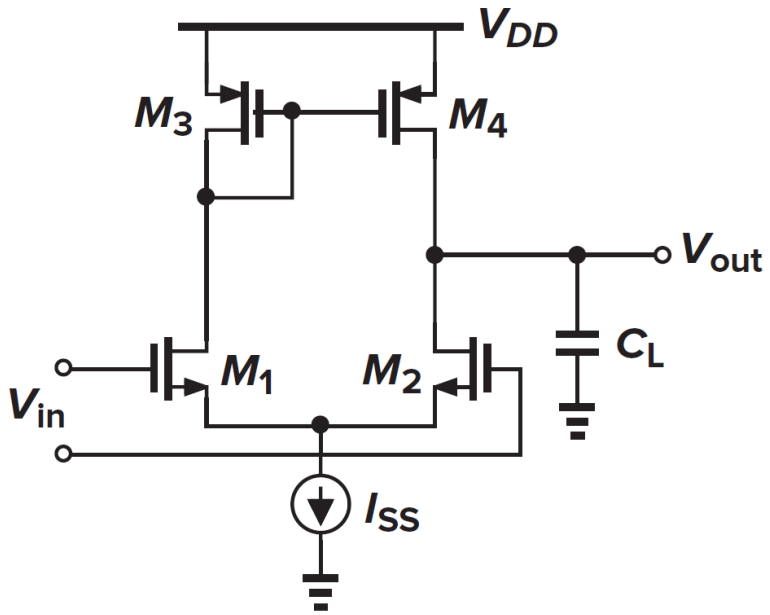

Figure 17: Differential pair with active load with a load capacitor attached at the output. Adapted from **[8]**.

2.3.5 New Keck Amplifier Operation

The Keck amplifier is a complex design that can be broken down into multiple, simpler pieces. Putting these pieces back together allows for a deeper understanding of the amplifier as a whole. This section seeks to describe the operation of this amplifier in a real situation. All node names and MOSFET names will be in relation to those seen in Figure 18. Node V_{IN+} will be assumed to be connect to some constant voltage source V_{REF}. Signal will arrive on V_{IN-} and the output will be sensed at V_{OUT}. The charge carriers will be assumed to be electrons, but the same ideas could be applied to a hole collecting device.

First, upon the arrival of the signal electrons, the voltage at the V_{IN-} node would decrease. This decrease would decrease the voltage at the gate of M_1 and the source of M_2. The voltage at the source of M_1 and the gate of M_2 is tied to V_{REF}, so it remains constant. These voltage changes

will lead to current changes in transistors M_1 and M_2 following $I_D = \frac{1}{2}\mu_P C_{OX}\frac{W}{L}(V_{SG} - V_{TH})^2$ where I_D is the drain current, μ_P is the mobility of the PMOS, C_{OX} is the oxide capacitance, W and L are the width and length of the transistor respectively, V_{SG} is the source gate voltage of the transistor, and V_{TH} is the threshold voltage of the transistor [8]. This change in current will increase the voltage at the drain of M_1 and decrease the voltage at the drain of M_2. This voltage change will change the operating conditions of M_5 and M_8. These transistors operate in saturation when idle, but they are in weak inversion. This means that while they are in saturation, they operate just above the $V_{DS} > V_{GS} - V_{TH}$ condition necessary to maintain saturation. The voltage change at the drain of M_8 can be enough to push this device into triode, and even cutoff turning it off. On the other side, M_5 would be driven into strong inversion and would sink more current. The differential amplifier with active load is formed by M_5, M_8, M_3, and M_4 so the two signal paths would both operate to drive the output voltage higher.

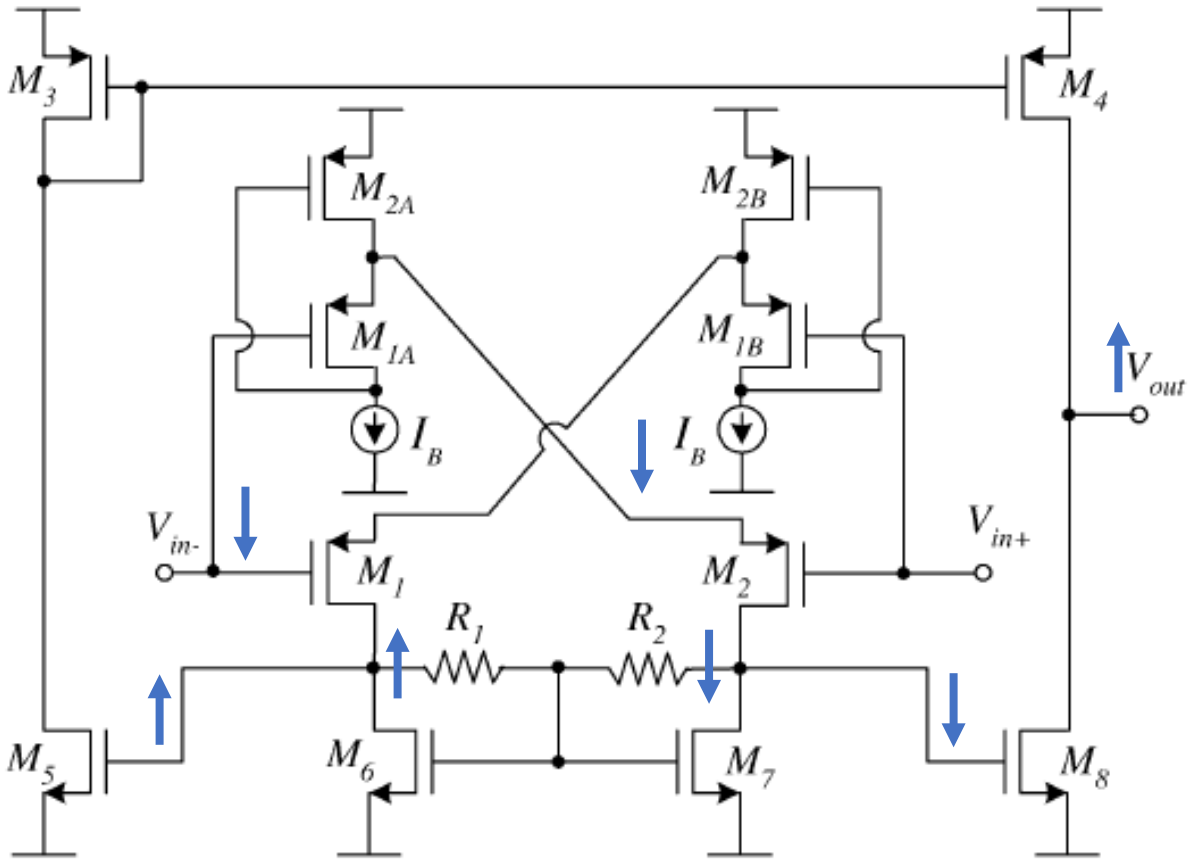

Figure 18: New Keck amplifier in an operational scenario. Changes in nodal voltage expressed via arrows. Adapted from **[9]**.

2.3.6 Keck 1 Amplifier Design

The amplifier utilized in the Keck 1 and Keck 2 is a class AB amplifier. This was designed by Carvajal et al. and adapted by Dr. Lucas Koerner to work in the Keck [10] [1]. This amplifier is designed to operate in class AB action. Class A action means that the device has a full bias current flowing at all times. This makes its small signal response excellent but its power dissipation poor. Class B devices flow no current when idle, but then increase the current when a load is sensed. This device has poor small signal response, but has excellent power efficiency due to the zero current flowing when idle. A class AB device combines the actions of both of

these architectures. It allows for the device to flow low, but non-zero currents at idle. The amplifier then increases the amount of current when a load is sensed. This gives this good small signal response and good power dissipation, with the low currents that flow when idle.

The class AB amplifier that was used in Keck 1 is pictured in Figure 19. This design is based off of the work done by Carvajal et al. but it does not use the local common-mode feedback (LCMFB) presented by this paper [9]. It instead opts for diode connected transistors at devices M3 and M4. This means that this amplifier achieves lower current gain than the designs made by Carvajal et al. While the adaptive bias current provided by the flipped voltage followers (FVFs) aid in making the device power efficient, it doesn't have the speeds required to be used in Keck 3. It was also designed on a 250nm 3.3V process meaning the transistors would need to be resized to work. This circuit was ruled out quickly during the design process.

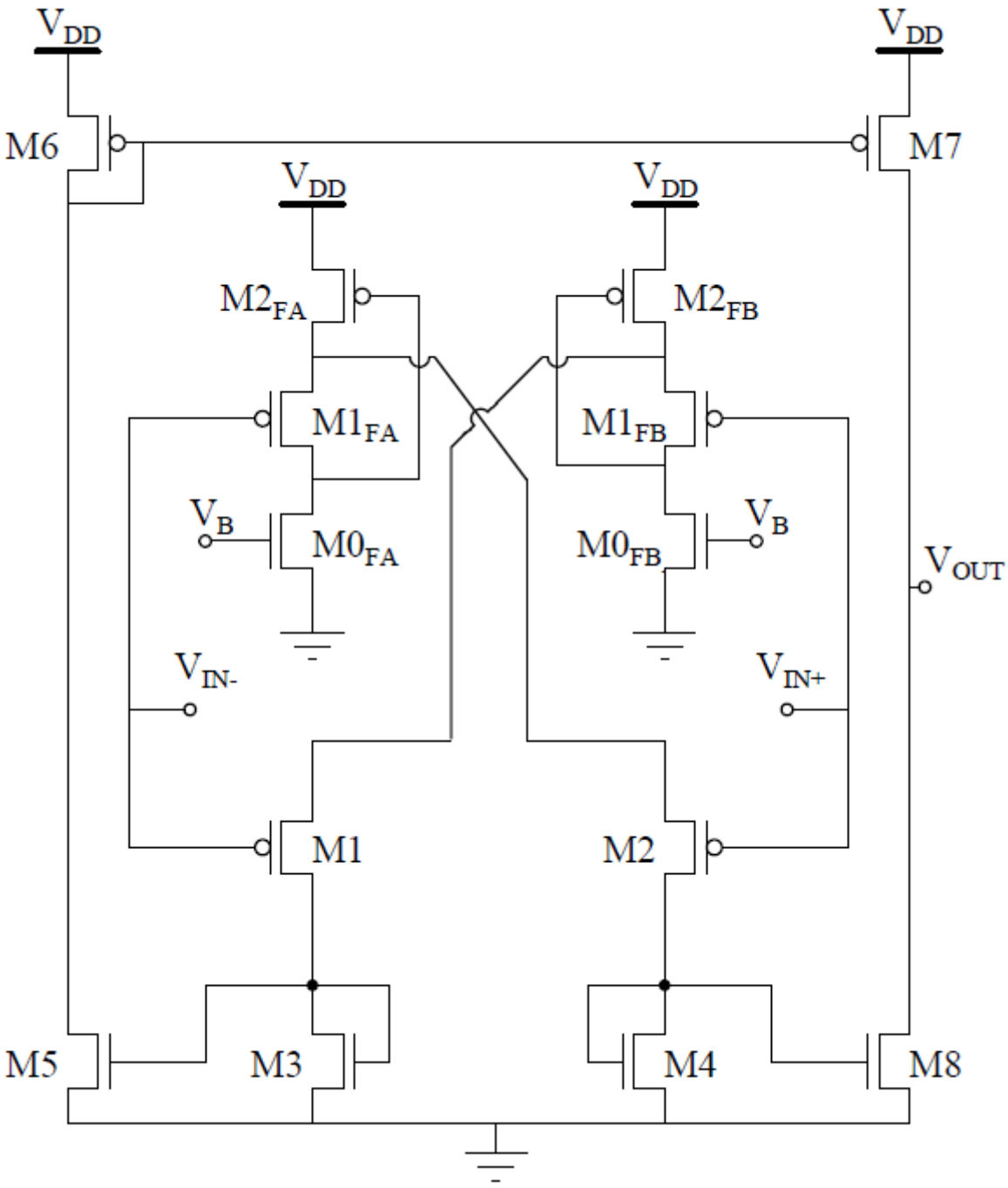

Figure 19: Class AB amplifier used in Keck 1. This design uses flipped voltage followers (FVFs) to provide an adaptive bias but it does not use the local common-mode feedback (LCMFB) presented by Carvajal et al. Adapted from **[1]**.

2.4 Switch Design

While not in the original scope of this project, time was spent looking at the design of switches. Switches have a significant amount of impact on the speed of the device, hence an investigation was deemed to be necessary. The designed circuit uses numerous switches that must be physically realized with transistors. The nonideal nature of the transistor switches cannot be ignored, so they needed to be designed to accurately test the performance of the amplifier. The ON resistance of the switches is a one such nonideal parameter. An ideal switch would have no resistance when closed and infinite resistance when open, but a transistor switch will have some small, but non-zero resistance when closed, and some large, but non-infinite resistance when opened. This resistance will also vary depending the drain-source voltage (V_{DS}). For that reason, care must be put into the design to ensure that the resistance is an acceptable level in all cases in which these switches are used. Other non-ideal aspects such as charge injection were briefly investigated, but not studied in depth.

Care must be taken when designing a transistor switch. First, the number and design of switches must be considered. A transistors switch could be designed with just a single transistor. This switch could be created from either an NMOS or a PMOS, and the voltage at the gate could be used to control the state of the switch. However, this switch has issues. One issue is that this design would not be resistant to a changing V_{DS}. If a single NMOS was used with a capacitor charged to V_{DD}, such as the design in Figure 20, issues would arise. If the signal at CK was to go from low (ground) to high (V_{DD}), the transistor would turn on in saturation, and the capacitor would begin to discharge following $I_D = \frac{1}{2}\mu_N C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2$ where I_D is the drain current, μ_N is the mobility of the NMOS, C_{OX} is the oxide capacitance, W and L are the width and length of the transistor respectively, V_{GS} is the gate source voltage of the transistor, and V_{TH} is the

threshold voltage of the transistor [8]. This equation will be followed until V_{DD} drops below V_{TH}, and the transistor enters triode region. This will decrease the current flowing through the device. As the drain-source voltage continues to drop, it will eventually drop to a point where the $V_{out} \ll 2(V_{DD} - V_{TH})$ and the MOSFET acts as a resistor, with resistance of $[\mu_N C_{OX} \frac{W}{L} (V_{DD} - V_{TH})]^{-1}$ [8]. The resistance when operating in this region will be significantly higher than the resistance when operating in saturation. Because of this changing ON resistance, a single transistor switch can be tough to implement. In summary, this switch has good ON resistance when a high voltage difference is sensed across it, but as the voltage difference comes closer to zero, its resistance increases.

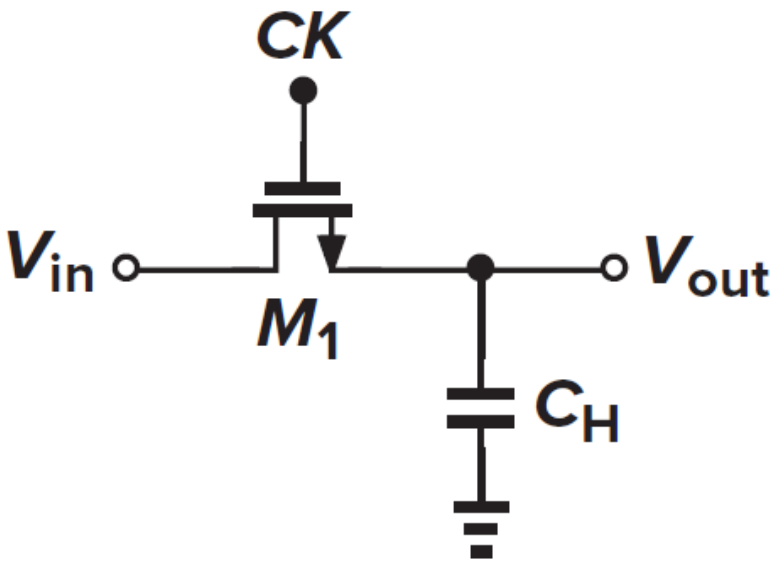

Figure 20: Transistor switch implemented using a single NMOS transistor. Capacitor C_H is used as a load device. Adapted from **[8]**.

The same non-ideal behavior would arise in a single PMOS switch, but some properties would be inverted to those of a single NMOS. Figure 21 is similar to Figure 20, but it uses a PMOS transistor in place of the NMOS. This figure again uses a capacitor that is charged to

some voltage, and the goal of the switch is to discharge this capacitor. The resistance of this switch would be very high for low V_{in} voltages, but it would be lower for higher V_{in} voltages.

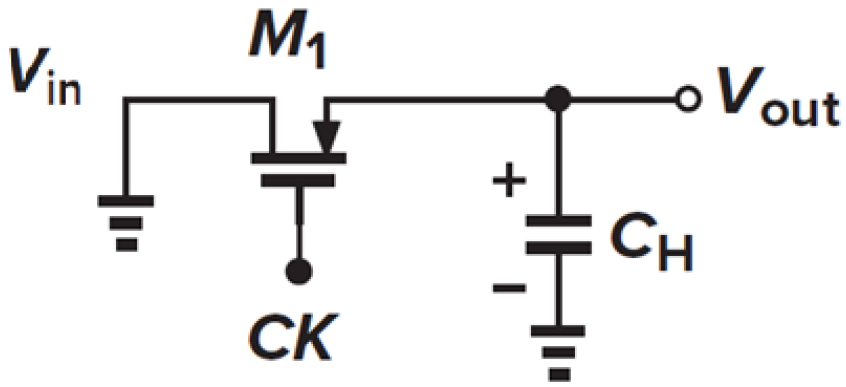

Figure 21: Transistor switch implemented using a single PMOS transistor. Capacitor C_H is used as a load device and can start charge to some voltage, or discharged. Adapted from [7].

The ON resistance of an NMOS and PMOS switch can be seen in Figure 22. This figure clearly demonstrates that an NMOS operates well for low values of V_{in} and a PMOS switch operates well for high values of V_{in}. These switches on their own struggle to behave uniformly across all levels of V_{in}, but each these switches both complement each other's behavior. A complementary MOSFET switch (also called a CMOS switch or a transmission gate) has been created. It uses and NMOS and a PMOS in parallel to allow for these devices to act together. This switch can be seen in Figure 23 [8].

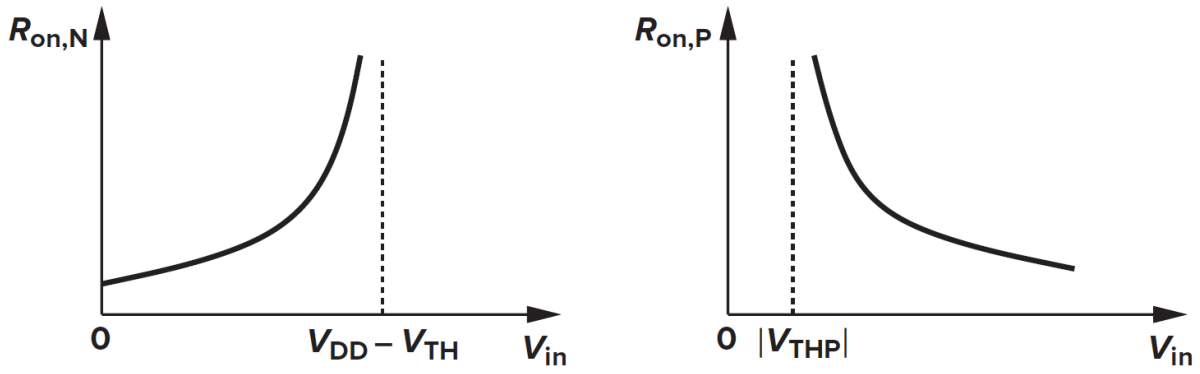

Figure 22: ON resistance of a single NMOS switch (left) and a single PMOS switch (right). Adapted from **[8]**.

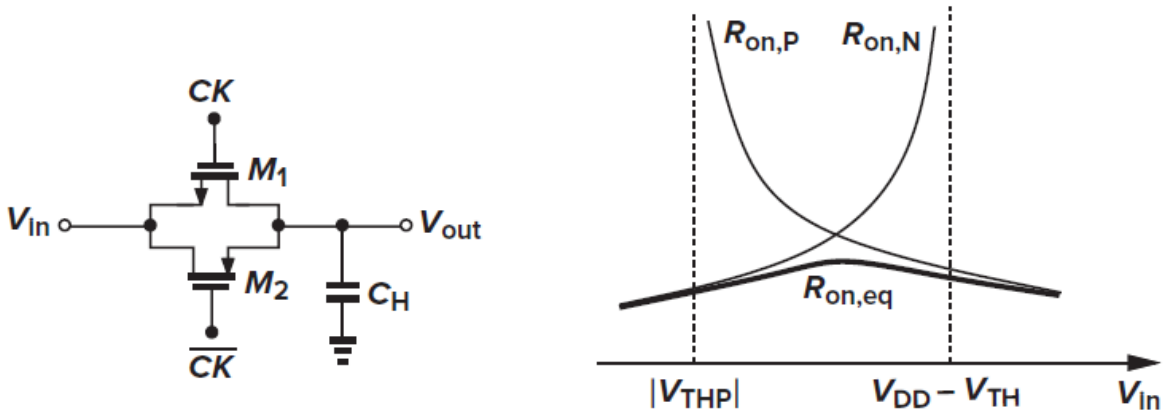

Figure 23: Transistor switch using CMOS to allow for low on resistance at all levels of V_{in}. Adapted from **[8]**.

The CMOS switch is the main design that has been investigated for this research. Its low ON resistance for all values of V_{in} allows for straightforward implementation into the pixel electronics. Some work was done investigating single transistor switch design, but the versatility of the CMOS made it stand out as the best candidate.

The design that was settled upon uses transistors with a width of 6µm and a length of 180nm for both the NMOS and PMOS. The SPICE code for these switches can be seen in Figure 24. This sizing was chosen for a few reasons. The main reason was simplicity. These switches have been used in previous successful designs so this sizing was a good place to start [2]. Since the focus of this project is amplifier design, switch design was an extra task that was only pursued due to necessity.

```
.subckt CMOS_Switch2 Clk Clkb Gnd Sw_IN Sw_Out Vdd
MM4 Sw_IN Clk Sw_Out Sw_Out nch W=6u L=180n AS=5.4p PS=13.8u AD=5.4p PD=13.8u
MM9 Sw_Out Clkb Sw_IN Sw_IN pch W=6u L=180n M=1 AS=5.4p PS=13.8u AD=5.4p
+PD=13.8u
.ends
```

Figure 24: SPICE code for chosen switches.

The CMOS switches that were choose have excellent ON resistance characteristics, which can be seen in Figure 25. This plot does not perfectly match the plot seen in Figure 23 due to differences in the mobility of the NMOS and PMOS transistor. This difference in mobility can be accounted for by changing the size of the switches. Instead of creating an NMOS and PMOS that are the same size, they could be created so that the ON resistance of the transistors is similar in their ideal environments. This would create the more symmetric style of plot like the one seen in Figure 23, but for the sake of time and simplicity, these switches were used.

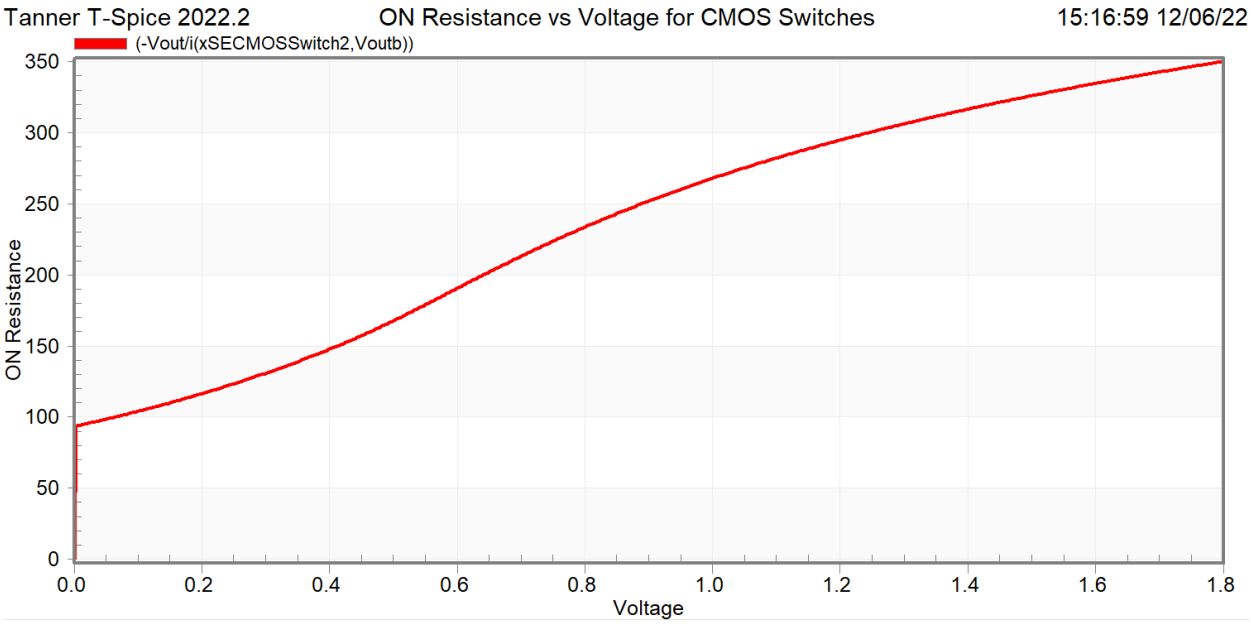

Figure 25: This graph shows how the ON resistance of the switches vary as the voltage applied across them is swept from 0V (ground) to 1.8V (V_{DD}).

These switches are not perfect. They are relatively large, meaning that it may be tough to physically implement them. Current designs also would require that the bulks of the transistors be electrically isolated, which would again be difficult to physically implement. They also have no way to mitigate the impact of charge injection, a phenomenon in which charge from the channel of a transistor is injected into the nodes attached to the source and drain. Since this pixel is made to count charge, this phenomenon is impactful and this switch design has no way of mitigating this. Despite these issues, these switches still exhibit excellent ON resistance, and they were used in all testbenches that involved switches.

3 Results and Conclusions

3.1 Transient Results

The most important results of this work are the transient results. As stated in 1.1, the most important parameter is the frame time of 77ns. If the detector is unable to take frames at 77ns, then it will be useless to the APS. Transient simulations have been conducted using SPICE simulations. Care has been put into insuring that these various testbenches have flexibility at their core, allowing for on the fly changes to parameters.

Transient test benches were constructed to match the drawing seen in Figure 26. The parasitic input capacitance is not shown in this figure, but it is created in the testbench. Two capacitors are used in place of C_F (called C_{INT} in Figure 26), both of which can be switched depending on the user's preferences. SPICE Parameters are used heavily in all testbenches for this research. Clocking assumed a 1 GHz clock, which is higher than what will physically be realized. The focus of this work was the amplifier design, so high clock speed was used for simplicity.

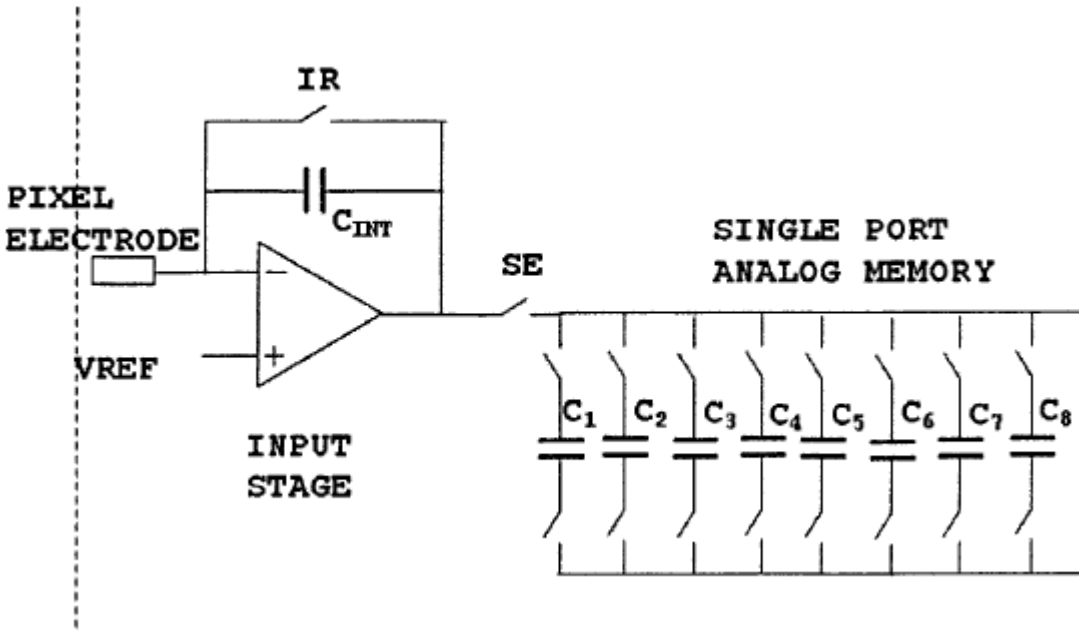

Figure 26: Simplified drawing of the Keck pixel electronics, where components like the amplifier and switches are represented as a symbol, rather than transistors. Not shown is the input capacitance on the pixel electrode. Adapted from **[3]**.

The input signal for this device is constructed simply from a current source. This current source is connected to the pixel electrode and a V_{DD}. The shape of the current source can be changed depending on the users input. The number of x-rays can also be set via user input. Five input shapes were test three of which are shown in Figure 27. The simplest is a square wave. This is useful for understanding the integrator behavior of the circuit. The second is a mostly unused exponential charge and decay shaped input. This was created early on to prove that the device could handle other shaped inputs, but it was not used often over other, more realistically shaped inputs. The third input is a 4-piece piecewise function. This approximates the input of a silicon sensor [11]. The fourth input is designed as 3-piece piecewise functions which simulates the input shape from a cadmium telluride sensor [5]. The last input is based of the fourth input, but it provides some randomness in the number of x-rays. All five of these inputs are designed to

simulate the arrival of 8 keV x-rays. These inputs only change the shape of the signal, and not the amount of charge delivered. In actuality, a cadmium telluride sensor will produce less electron-hole pairs than a silicon sensor, but this would require resizing of the capacitors, and the original projects was based around a silicon sensor. While a system to change the size of the capacitors depending on the input type is possible, it was thought to be not the best way to realize this.

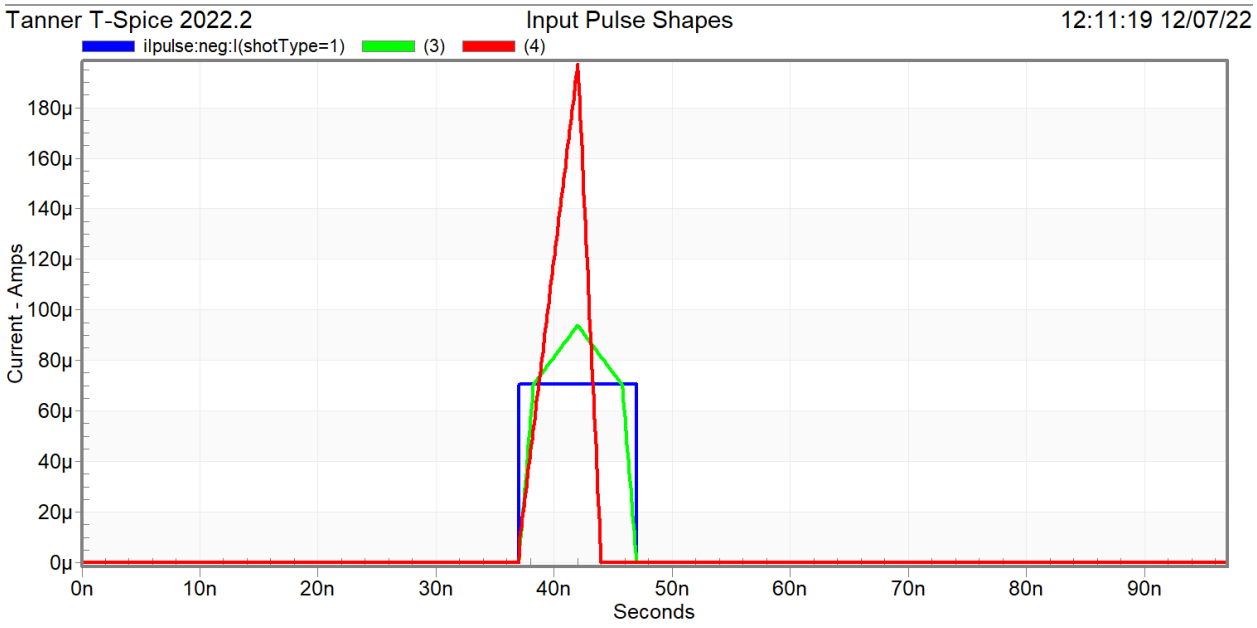

Figure 27: This graph shows different input pulse shapes used to test the amplifier. The blue is a simple square wave. The green curve approximates the input for a silicon sensor **[11]**. The red trace approximates the input for an electron collecting cadmium telluride sensor **[5]**.

Figure 28 shows a complete shot and the beginning of the next shot, with the distinct temporal windows indicated on the figure. First, the pixel must switch in a storage capacitor. Then, the reset switch is closed around the amplifier, clearing any charge of the feedback capacitor and any residual charge that may have accumulated on the storage capacitor. Next, the device integrates the incoming charge to complete the shot. The instantaneous response of the capacitors

causes the jump seen at 37ns, but clear integration behavior can be observed at about 42ns. The pixel then settles, and the 77ns time is clearly indicated, showing that this device can make the requisite 77ns speeds. The next shot then begins, switching out the first storage capacitor and putting in the next. The pixel then resets, and integration would ensure.

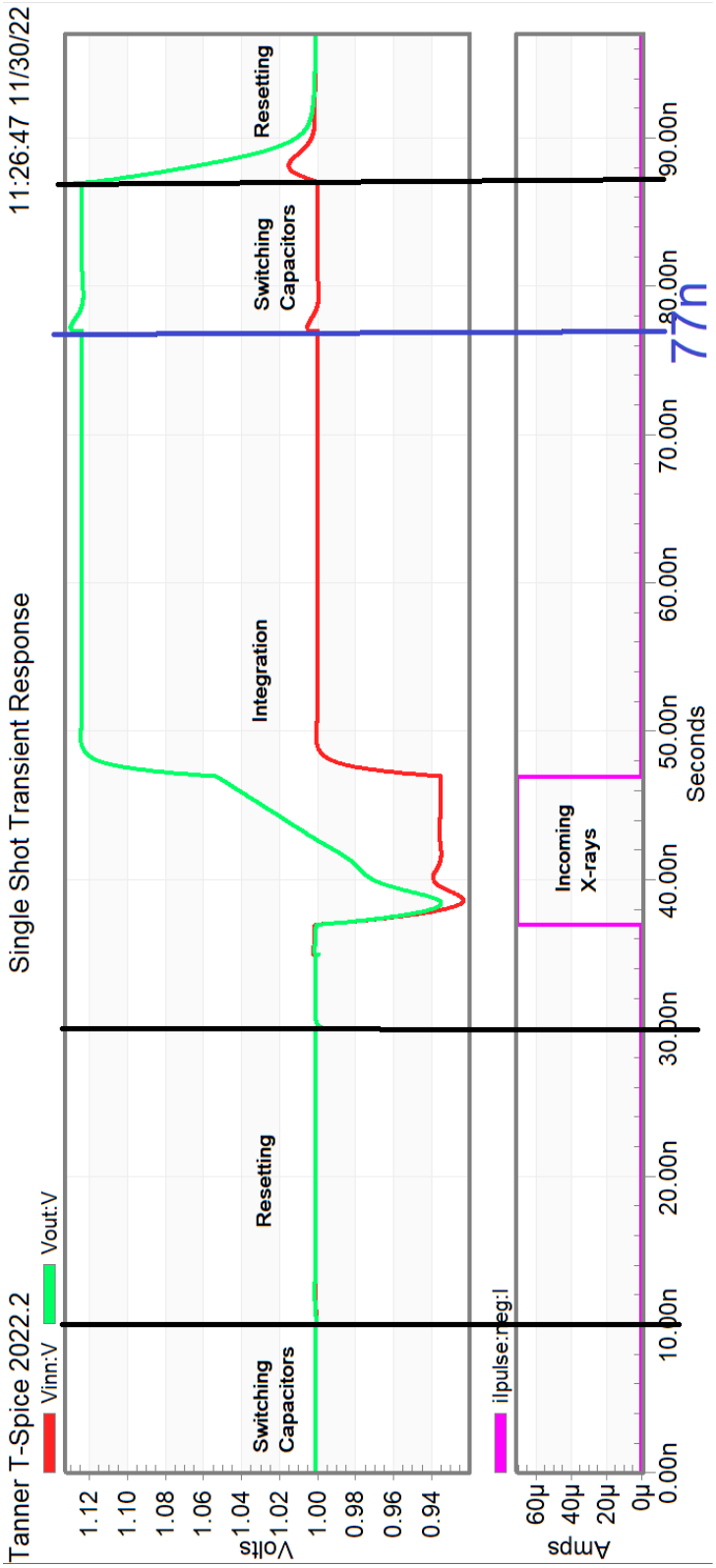

Figure 28: This figure shows pixel electronics in use with the different temporal windows of a shot noted on the graph.

Through thorough parameterization, a single transient testbench can be modulated to provide dozens of useful results. Firstly, it is able to respond to different numbers of x-rays. This number of x-rays can be set by a user, or it can be produced by using a random input, which can be seen in Figure 29. The size of all capacitors can be changed, and the dimensions of all transistors in the amplifier can be changed. All timing parameters can be changed, and as stated previously the input shape can be changed. In general, any numeric value in this design is set as parameter. This flexibility has been instrumental in the usability of this testbench allowing for dozens of different results to be collect.

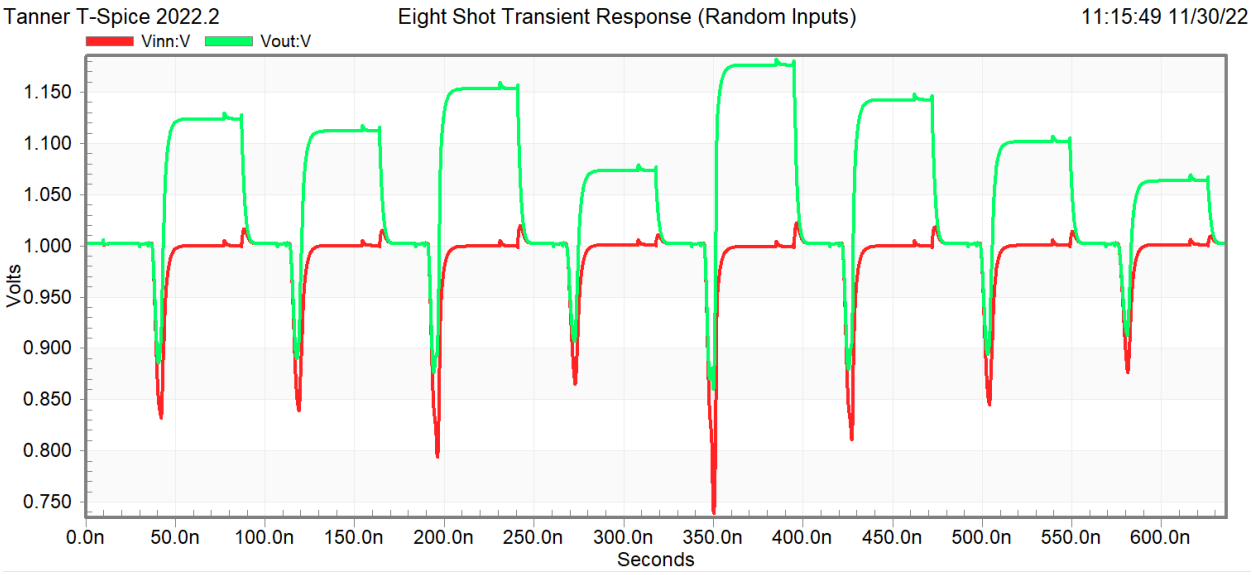

Figure 29: Input (red) and output (green) voltages of the amplifier when random inputs are sent into the Keck pixel.

The input and output voltage trace for eight shots can be seen in Figure 30. Here the input current can also be seen, and all eight pulses are the same. This figure (and Figure 29) shows that the device can handle the 77ns speeds that are required of it. The temporal windows of Figure 28 can clearly be seen in the traces of this figure. The output settles in time, and its accuracy can be

seen in Figure 31. This device is producing the correct output for all values within its range. With a cadmium telluride shaped input, some issues arise which can be seen in Figure 32. The device is not accurate past 7,000 8 keV x-rays. These issues are easily explained. First, the scenario present in Figure 32 is not a realistic scenario. As stated prior, the cadmium telluride input pulse shape is only a shape. It still has charge values of a silicon sensor. To change the amount of charge being integrated, the feedback capacitors would need to be changed by a proportional amount. If this device was creating an accurate amount of electron hole pairs for the sensor material, it would be accurate up to 8,000 8 keV x-rays. It is important to note that there is some charge injection which must be offset to read out accurate x-ray values from the storage capacitors, but that is physically realizable. An FPGA could have an offset programed in.

Work to improve the gain of this system is discussed in section 3.2. Utilizing the methods seen there the DC gain of the amplifier can be improved without increasing the power draw. This gain boosting technique improves the transient response as well. The gain boosted transient response can be seen in Figure 33. There is some slight overshoot, due to the systems poles becoming slightly imaginary, but this tradeoff is ultimately worthwhile.

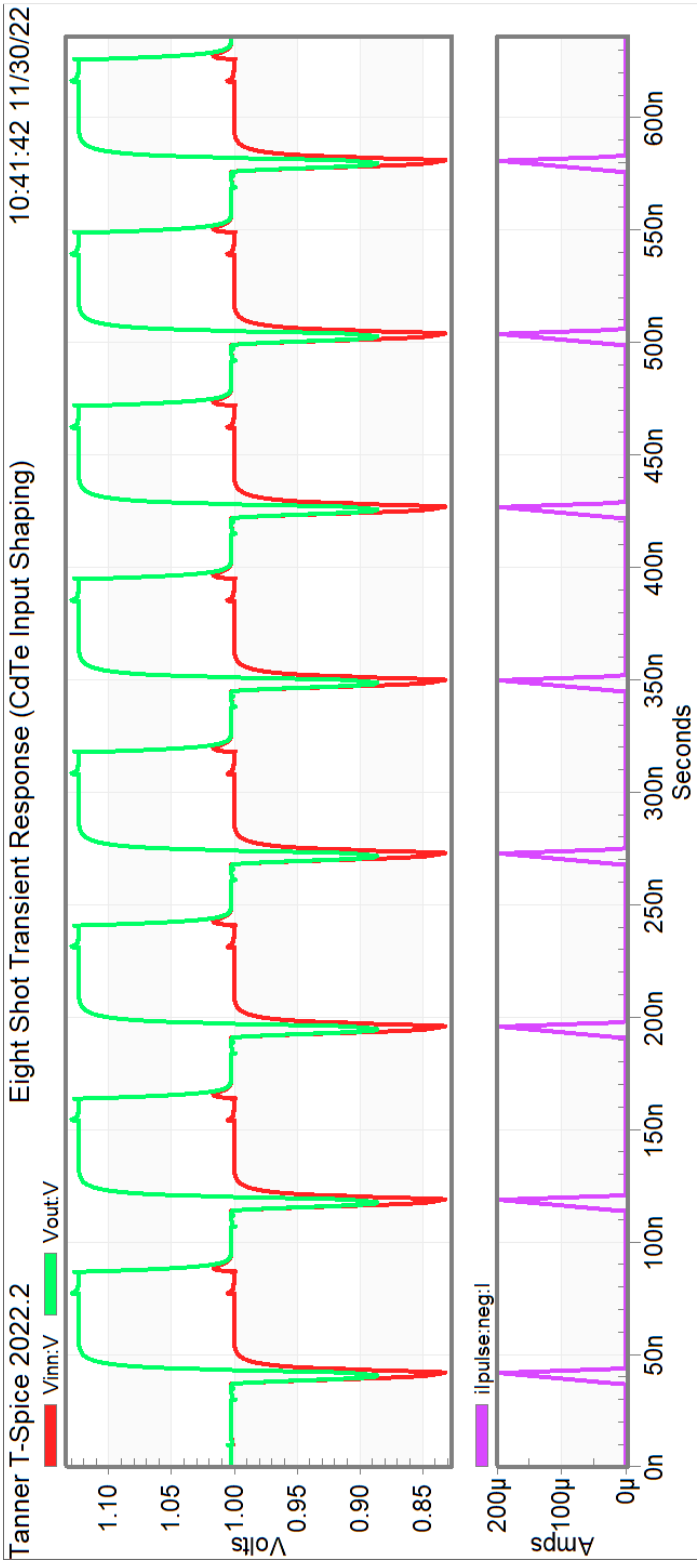

Figure 30: Response of the pixel electronics for eight shots. The input current source (seen in purple) is shaped to model that of a cadmium telluride sensor.

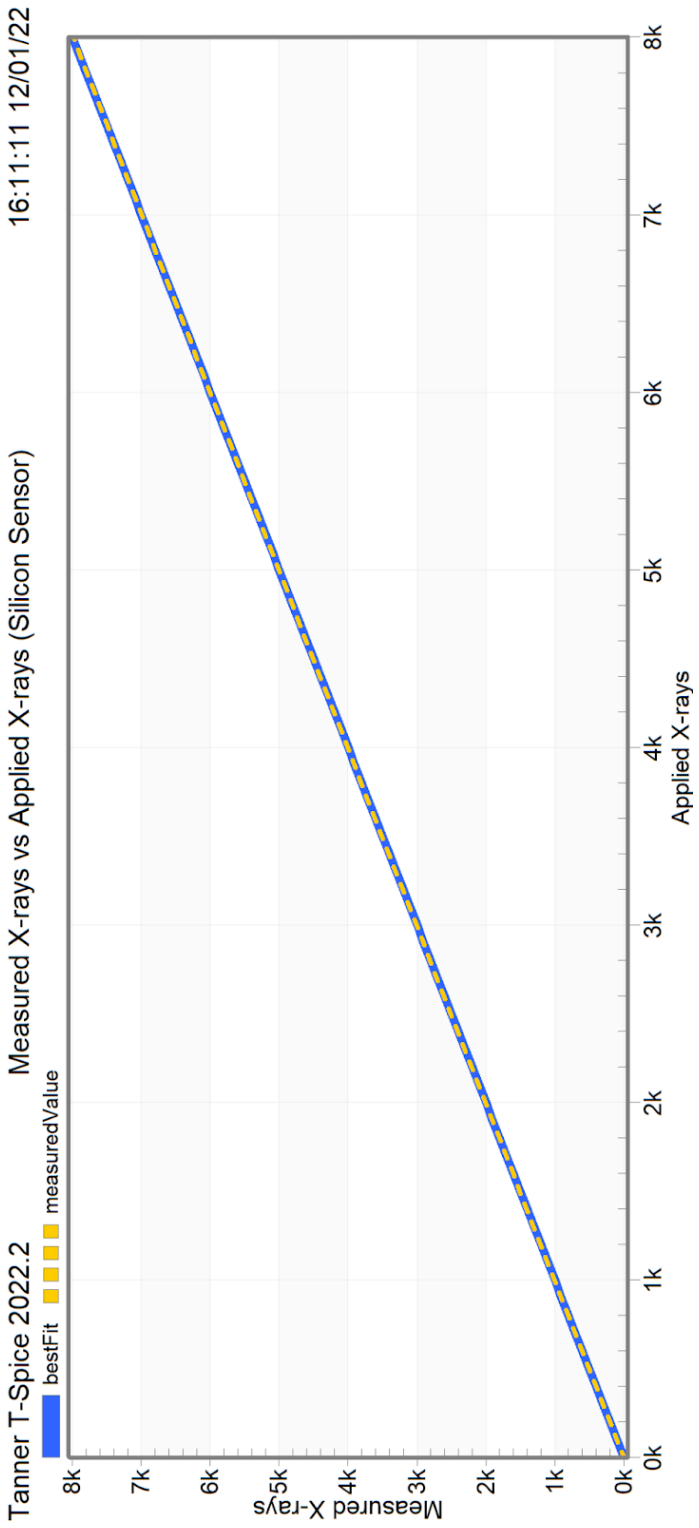

Figure 31: This plot shows a y=x line in blue, and the output value (in x-rays) of a storage capacitor after a shot using a silicon pulse shape has been taken in dashed yellow. This shows that the device is accurate for all values in the designed for range of 8,000 8 keV x-rays.

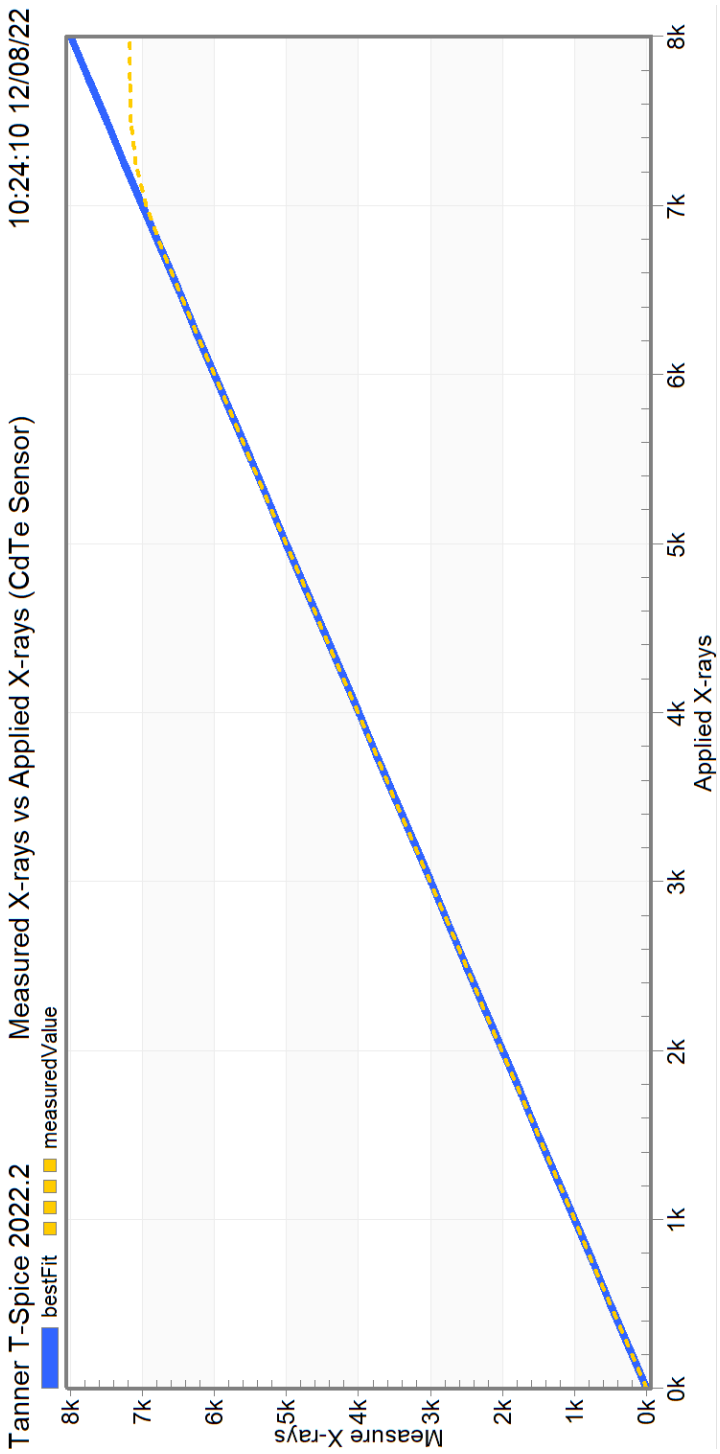

Figure 32: This plot shows a y=x line in blue, and the output value (in x-rays) of a storage capacitor after a shot using a silicon pulse shape has been taken in dashed yellow. This shows that the device is accurate for all values in the range of >7,000 8 keV x-rays, but the system is unable to accurately produce results past approximately 7,000 x-rays.

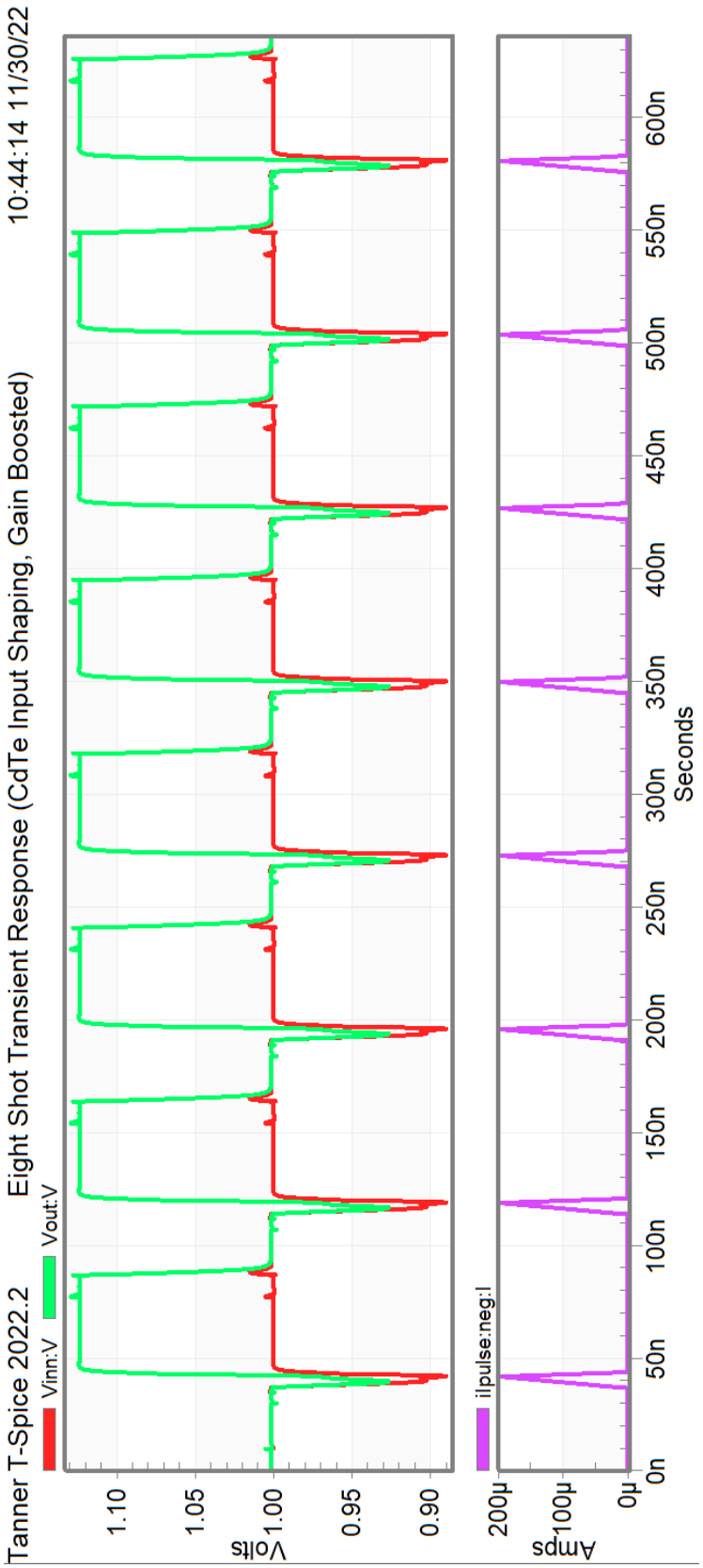

Figure 33: Transient results with an increase in the DC gain of the amplifier.

3.2 AC and Noise Results

The AC characteristics of this amplifier and the noise characteristics are presented here. AC parameters such as DC gain and phase margin are important to this device. The DC gain has impact on the charge collection efficiency and reset (pedestal) voltage levels. It is beneficial to maximize the DC gain of the device. Phase margin is an important characteristic to maintain stability in the circuit. Phase margin relates to the feedback of the device. The feedback should be inverting, but due to delays in the circuit, there may be some change in phase. This can lead to oscillation instead of a controlled integration. Noise is an important parameter that designers must seek to minimize. Noise can arrive from devices in the circuit, or from external sources such as clocking noise. In this work, only the amplifier noise was investigated. The noise accumulated on capacitor was also briefly studied, but it was deemed to be significantly less than the amplifier noise.

SPICE has AC simulations built into it allowing for easy generation of Bode plots. These Bode plots can be used to find the DC gain and phase margin of the amplifier. While the generation of Bode plots is simple, designers must take care to ensure that the circuit being tested is designed properly. Open loop parameters are important in AC simulation, and the loop must be opened properly to get accurate results. In this case, the amplifier is sensing a voltage and returning a current so the feedback load should be duplicated and both sides grounded. This is depicted in Figure 34. A Bode plot gathered from this simulation is shown in Figure 35. These plots show a DC gain of about 35.5dB (about 61 V/V) and a phase margin of 89.5°. The DC gain is low, but the phase margin is phenominal. The DC gain of the original Keck was about 500 V/V, so this is significant decrease in DC gain, but this amplifier design has worked in previous PADs [2]. The phase margin of this amplifier is phenomenal. A critically damped system would have 90° of

phase margin. Any system over 60° of phase margin is acceptable, so room exists to improve the DC gain of the amplifier at the cost of phase margin [8].

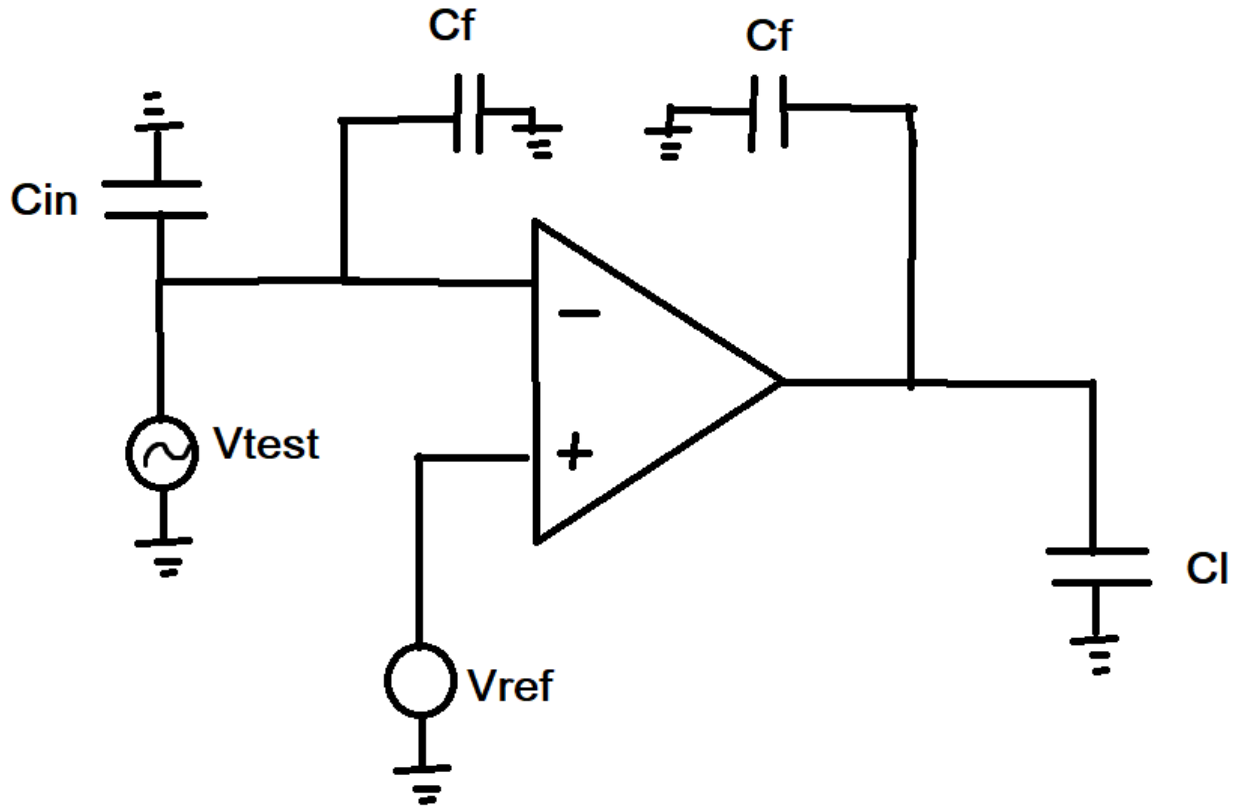

Figure 34: Visualization of the circuit used to test AC characteristics.

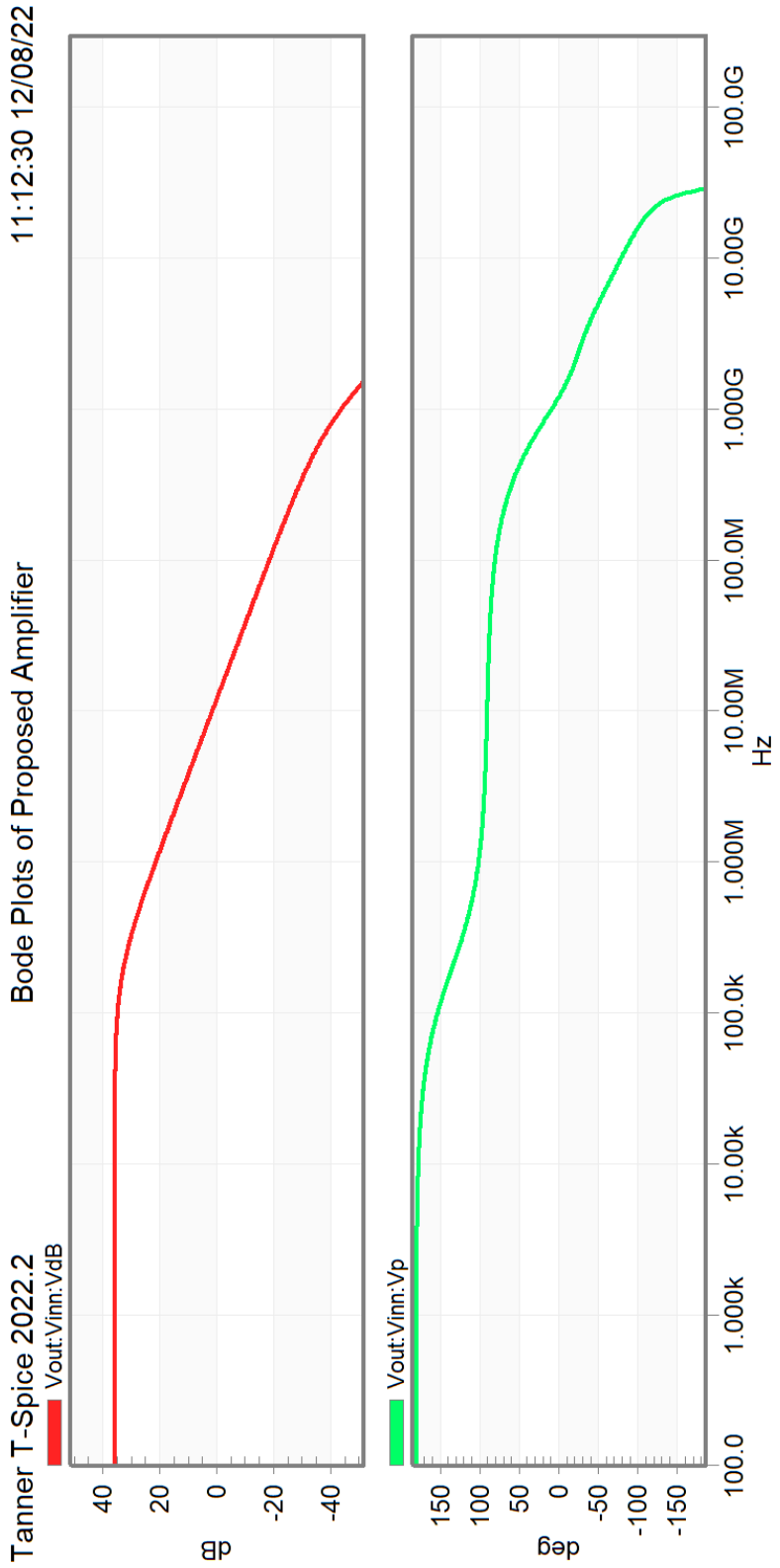

Figure 35: This figure shows the Bode plots of the proposed amplifier with its default transistor sizing.

There are very simple ways to improve the DC gain of this system. The most fruitful has been increasing the size of the M_1 and M_2 transistor pair (see Figure 14). Transistors M_5 and M_8 also effect the gain, but the effects were found to be insignificant (netting only 1dB at the cost of unacceptable levels of power consumption. Increasing the width of transistors has been implemented in SPICE as a multiplier on the existing size. The results of this sizing change are shown in Figure 36. This pair has significant impact on the gain of the device, but it also has an impact on the power draw as can be seen in the top portion of this table. This increase in idle power is unacceptable, even at the 2x level. To compensate for this, the bias current can be decreased proportionally to the increase in width, yielding the results in the second half of this table. Gain is increased significantly (about 110 V/V at the compensated 5x multiplier). This comes not at the cost of power but phase margin. Before this device was nearly critically damped, with a phase margin of 89.5°, but as the width increases, the phase margin decrease. However, this decrease is not significant. At a 5x multiplier, the phase margin only drops to 83.0°, which is noticeable, but not impactful. This phase margin will manifest some slight overshoot and ringing in the system, but it comes at the results of significantly improved gain, which is a tradeoff that must be made.

	$W_{M1\&M2}$ = 0.5x	$W_{M1\&M2}$ = 1x	$W_{M1\&M2}$ = 2x	$W_{M1\&M2}$ = 3x	$W_{M1\&M2}$ = 5x
Width (µm)	600nm	1.2µm	2.4 µm	3.6µm	6.0µm
DC Gain (dB)	29.08	35.50	41.00	43.76	46.70
Phase Margin (degrees)	91.5	89.5	85.7	80.9	68.9
Idle Power (µW)	55	88	150	206	309
With bias current turned down to accommodate the increase in size of transistors					
DC Gain (dB)	32.3	35.5	38.2	39.5	40.9
Phase Margin (degrees)	90.6	89.5	87.9	86.3	83.0
Idle Power (µW)	93	88	82	81	82

Figure 36: Results from changing the width of M_1 and M_2.

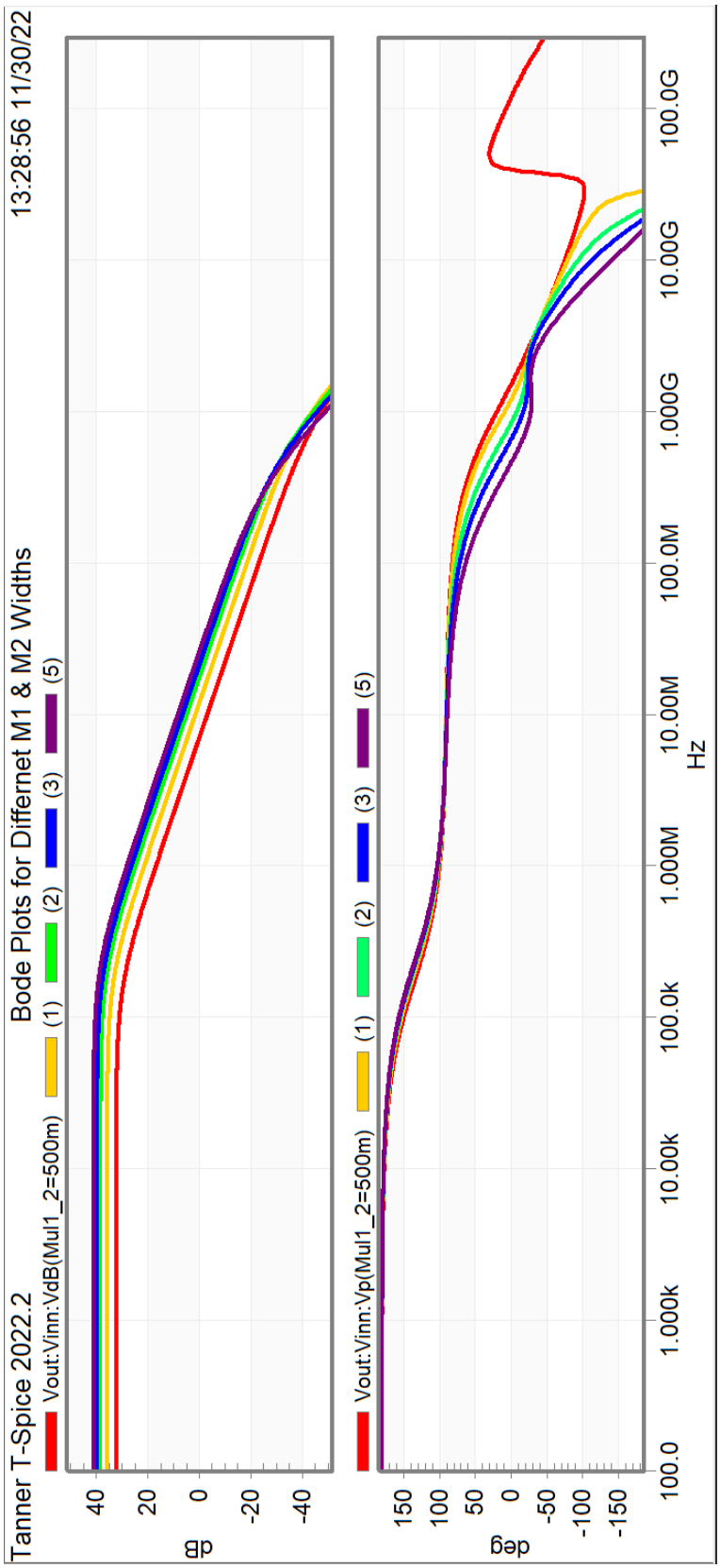

Figure 37: Bode plots used to gather the results in **Figure 36**.

SPICE has simulation commands specifically for noise. This command is run over an AC simulation but the configuration of the device is changed slightly. In a noise simulation, feedback is not removed, and a large inductor is used to help the simulator solve for DC points without changing the AC properties. This simulation was mostly created primarily by following in the footsteps of previous PAD testbenches. The plot of the results can be seen in Figure 38. This plot can conclude that at 50MHz, a 50fF capacitor (71 8 keV x-ray full well) would experience about 0.20 8 keV x-rays of noise, 844fF capacitor (1200 8 keV x-ray full well) would experience about 1.13 8 keV x-rays of noise, 5632fF capacitor (8000 8 keV x-ray full well) would experience about 6.42 8 keV x-rays of noise.

This noise is acceptable and is in line with previous PADs [1]. It is not in line with the deliverables of this project. The deliverables indicate that noise of less than 1 8 keV x-ray should be present at the high gain (844fF) capacitor, but this is not met. This is due primarily to a failure to understand the task, leading to unreachable goals being set. Small capacitors, like the 50fF tested here are where low noise can be expected. The MMPAD 2.0 gets low noise of less than an 8 keV x-ray from 40fF capacitor, not from the full 880fF [2]. Due to inexperience, the bar was set much too high, and this goal was unachievable.

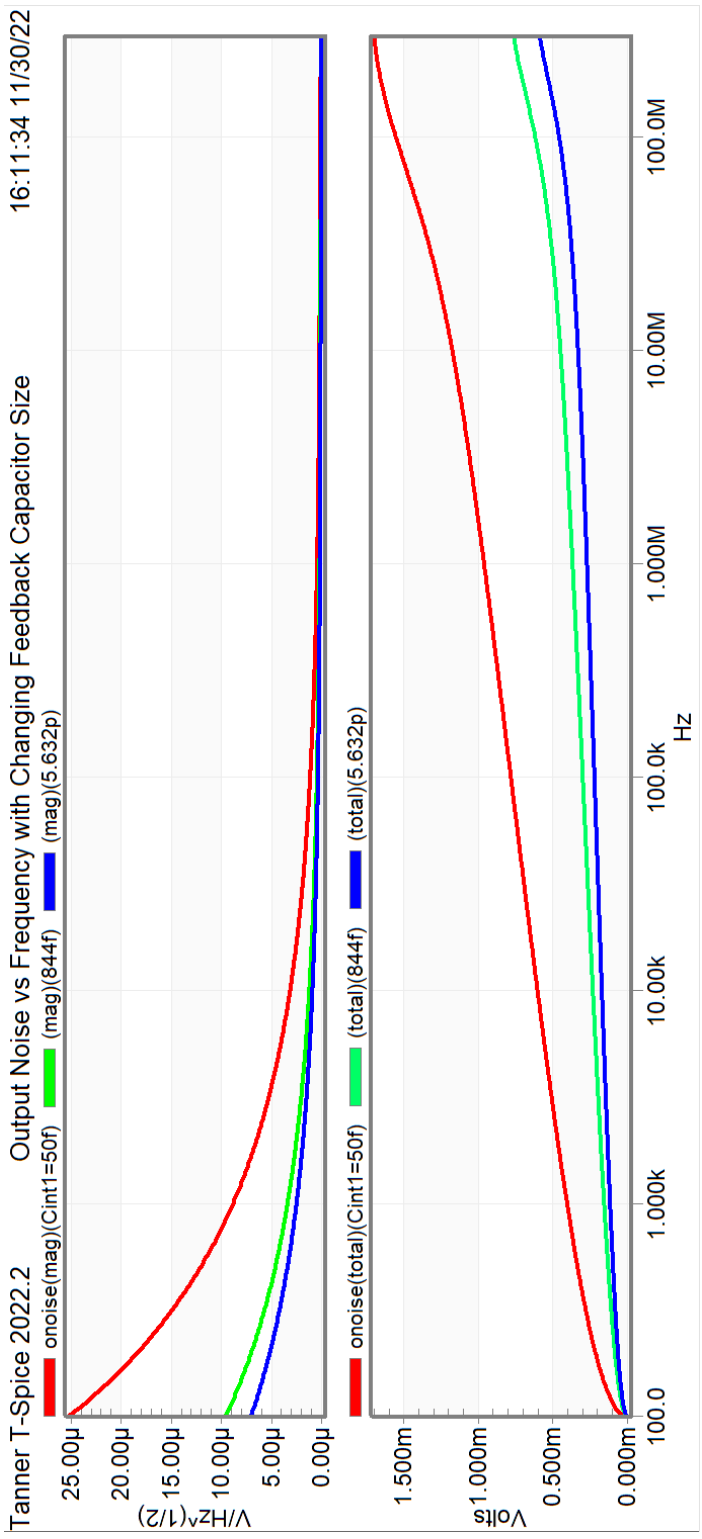

Figure 38: Output noise of the amplifier for different sizes of feedback capacitors.

3.3 Slew Rate

The slew rate of this amplifier is straightforward. The slew rate is dependent on the size of the output capacitor and the amount of current that the amplifier can provide to said capacitor. To find this current, the amplifier is put into the setup seen in Figure 39. The noninverting input of the amplifier is connected to a reference voltage V_{REF}. The inverting input is connected to the output via a wire. A small resistor connects the output of the amplifier to two voltage sources, one that is a static reference voltage V_{REF} and another voltage that can be change be used to create a voltage difference between the two input V_{DIFF}.

Results from the Figure 39 setup are shown in Figure 40. This graph shows that the output current of this amplifier is large for any voltage difference over |0.2V|. It also shows that the output current is not linear, and it isn't symmetric. For values greater less than -0.2V, the output current is about -250µA, but for values greater than 0.2V the output current is about 450µA. This asymmetry means that the amplifier would be able to handle more x-rays in a hole collecting device, where positive voltage differences are expected at the input.

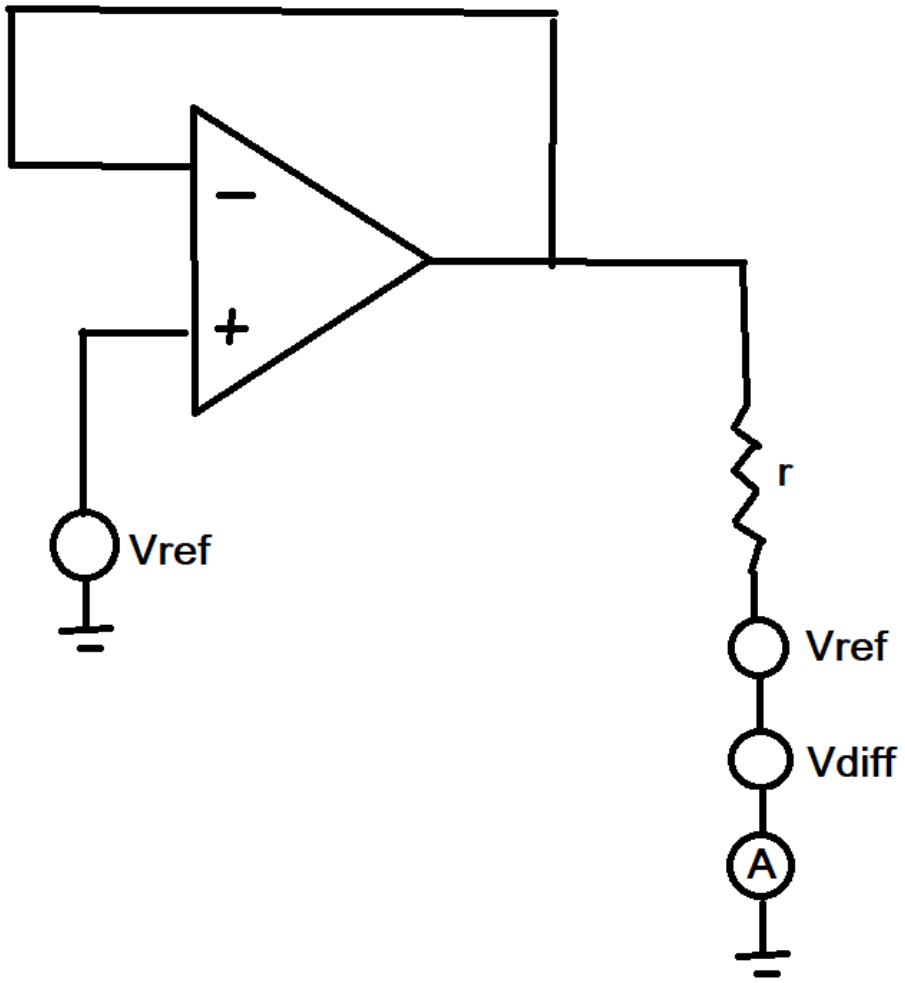

Figure 39: Visualization for the testbench used to find slew rate.

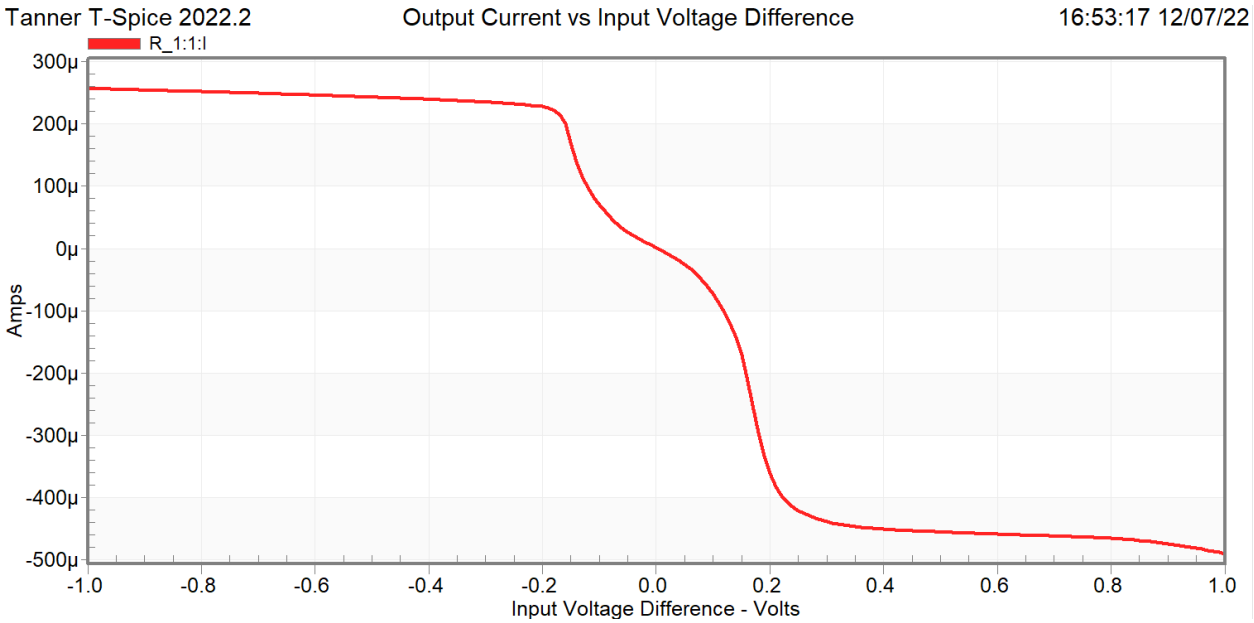

Figure 40: Pictured is the output current of the amplifier when a small resistor is attached. This current can be used to find the slew rate of the amplifier.

3.4 Conclusions and Future Work

According the simulations presented, this circuit will be able to make the 77ns speeds. Transient simulations show that the device will be able to take 8 shots, in 77ns while maintain low idle power. The device is able to process 8000 8 keV x-rays, and a working device has been created on the 180nm architecture. The device is still low power, with the average idle power of about 85µW. However, the noise is higher than what was promised. This is due to a lack of understanding when laying out the deliverables, leading to overpromises in noise. The device cannot process single x-rays at its current high gain setting.

Moving forward, there is plenty of work to be done. The DC gain of the amplifier is low, even when the width of M_1 and M_2 are increased. This can lead to inconstancies from pixel to pixel. It can also create a bevy of other issues, such as inaccurate results, improper resets, and

poor charge collection efficiency. This parameter is very important to amplifier design, and improved DC gain is of much interest to this work.

Power droop has also been largely ignored in this research, but it is an issue that will crop up if not properly accounted for. The wire bonds for this chip only come in from one side, so V_{DD} and ground can "droop" across the chip due to the nonideal conductor that their rails are formed from. This can lead to the voltage of V_{DD} decreasing across the chip, and the voltage of ground increasing. Thanks to the thorough parameterization of testbenches, these effects have been briefly investigated and were deemed to be impactful. This is something that will need to be designed for, and will garner a full investigation in the future.

Due to the unsatisfactory noise performance of the chip, adaptive gain should be considered for this device. Adaptive gain changes the feedback capacitance during integrations, allowing for a small, low noise full well to be used initially. If the input hits some threshold, then an additional capacitor can be put in, changing the full well an allowing the device to continue integration. This system has been successfully implemented in the MMPAD 2.0, and was one of the reasons that the new Keck PAD has begun using the 180nm process [2]. This system from the MMPAD can be carried over to the Keck, allowing for very easy implementation.

As stated in section 2.4, the switches in this circuit will need some work. They are large, and that are not able to mitigate any charge injection. A smaller switch is desirable, but that would come at the cost of increasing the ON resistance of the switch.

Lastly, a test chip must be created and fabricated, to test the actual performance of this device. This is a lengthy and expensive process, but it is the best way to actually test the performance of this device.40

Idle Power	> 100µW
Full Well (low gain)	8000 8-keV x-rays
Full Well (high gain)	1200 8-keV
Noise (high gain)	1.13 x-rays
Minimum Frame Time	77ns
Transistor Process	TSMC 180nm 1.8V

Figure 41: Deliverables

4 References

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