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Pixel array detector for the capture of femtosecond duration x-ray images (Paper Presentation)

Paper 6703-22 of **Conference 6703**

Authors(s): Hugh T. Philipp, Lucas J. Koerner, Marianne Pouchet, Mark W. Tate, Sol M. Gruner, Cornell Univ.

Date: **Monday, 27 August 2007**
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First results from the 128×128 pixel mixed-mode Si x-ray detector chip (Paper Presentation)

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Authors(s): Wayne Vernon, Matt Allin, Ron Hamlin, Tom Hontz, Doan Nguyen, Area Detector Systems Corp.; Xuong Nguyen-Huu, Univ. of California/San Diego; Frank L. Augustine, Augustine Engineering; Sol M. Gruner, Daniel R. Schuette, Mark W. Tate, Lucas J. Koerner, Cornell Univ.

Date: **Tuesday, 28 August 2007**
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Pixel Array Detector for the Capture of Femtosecond Duration X-ray Images

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ABSTRACT

An imaging Pixel Array Detector (PAD) is being developed to record x-ray scattering images from single particles at the SLAC Linac Coherent Light Source (LCLS) x-ray free electron laser. The LCLS will deliver x-ray pulses of 5 – 200 femtosecond duration 120 times per second. Proposed experiments require that the scatter from each pulse be independently recorded. This necessitates a detector with a charge integrating front-end because the high instantaneous arrival rate of photons (> 1000 photons per pixel in femtoseconds) exceeds the processing speed capabilities of digital counting detectors. Other capabilities of the PAD are a frame rate >120 Hz, a full-well depth in excess of 2000 8-keV photons, a detective quantum efficiency near unity, and the ability to readily differentiate between 0 and 1 photons per pixel. The detector will be a 4x4 array of subunit tiles. Each tile consists of two silicon chips solder-bump bonded together. A pixelated 500 micron thick, fully depleted silicon chip converts x-ray energy into charge carriers. The charge created is conveyed by solder connecting bumps to a CMOS ASIC in which each pixel has its own signal processing electronics. Each tile has ~190 x 190 pixels, resulting in a detector of > 760 x 760 pixels. Tests of prototype 16x16 readout pixel arrays show a read noise equivalent to 0.14 8-keV photons. Features of the detector include an in-pixel parallel 14-bit digitization scheme, and the capability to be configured with an adaptable, 2-level, 2D gain profile. The development of the read-out electronics and the effects of tiling on dead area are also discussed.

Keywords: x-ray, xfel, cmos imager, pixel array detector, radiation detector

1. INTRODUCTION

The idea behind the single particle scattering experiment proposed for the LCLS is explained in[1]. The experiment will inject lone biological particles into a vacuum chamber every 8 ms. These particles will interact with a femtosecond pulsed x-ray beam. The extreme intensity of the x-ray pulse will ionize the particle being studied, causing a destructive coulomb explosion of the particle. If the time scale of the x-ray pulse is shorter than that of the momentum limited coulomb explosion, the scattered x-rays will reflect the electron density of the molecule's original structure (i.e. the structure of the molecule before it is destroyed). This allows for the possibility of determining the structure of a single particle without crystallization.

Since the orientation of the particle interacting with the x-ray beam will be unknown, the collected scattering patterns need to be analyzed and organized into groups of images representing similar orientations. Computational simulations show that the faithful detection of the few scattered photons in the high 2θ regime, where θ is the angle between the scattered radiation and the direct beam, are crucial for the determination of the particle orientation. This translates into the requirement that the detector has a read-noise of less than a fraction of a photon[2]. Simulations also predict scattered signals of ~ 2000 x-rays in pixels nearest the incident beam. The need to both detect 2000 x-rays per pixel and to have readout noise equivalent to less than a fraction of a photon, defines the required dynamic range of the detector.

While the instantaneous rate of photons arriving at the detector face of highly illuminated pixels may approach 10^{17} photons s^{-1}, the signal arrival rate at the readout chip is limited by the drift velocities of holes. The time it takes to collect all the charge in the detector layer depends on the voltage bias across the diode and is generally on the order of 10's of nanoseconds, which implies arrival at the readout chip may exceed ~10^{11} photons s^{-1}. The reported maximum count rate of standard digital counting PADs is ~10^7 photons s^{-1}. This indicates an analog integrating front-end is needed for the experiment[3,4].

Ultrafast X-Ray Sources and Detectors, edited by Zenghu Chang, George A. Kyrala, Jean-Claude Kieffer,
Proc. of SPIE Vol. 6703, 67030O, (2007) · 0277-786X/07/$18 · doi: 10.1117/12.733866

The readout rate of 120 Hz prevents the use of phosphor-coupled CCDs because of potential problems with phosphor afterglow, while the desired saturation value of >2000 photons and rapid readout time make finding a proper direct illumination CCD difficult. A CMOS based PAD is an excellent solution for the experimental demands because it can meet both the 120 Hz frame rate, and high dynamic range requirements. PADs also display superb point spread behavior[5,6] .

2. DETECTOR OVERVIEW

The PAD is constructed as a hybrid of two distinct layers. The first layer is a high-resistivity, 500μm thick, fully-depleted, reversed-biased, pixelated, silicon diode layer where x-rays are absorbed and converted to electron-hole pairs. The second layer is a readout chip fabricated with conventional complementary metal-oxide semiconductor (CMOS) electronics using a commercial 0.25 micron mixed-mode process. Both the detector and readout chips are pixelated with single pixel dimensions of 110 μm by 110 μm. The pixels of the detector diode layer and the CMOS layer are connected with bump-bonds through which the holes generated by x-rays absorbed in the diode are conveyed to the CMOS processing electronics.

2.1 CMOS readout chip

The CMOS readout chip pixel uses a capacitive transimpedance amplifier (CTIA) as a charge integrator and to maintain a stable electrode voltage at the input. X-ray induced photocurrent produces a voltage change at node A shown in Figure 1. The charge-to-voltage gain of the CTIA may be programmed in each pixel using in-pixel one-bit memory to select the feedback capacitance. Two gain settings are available by setting the feedback capacitance to be either 75 fF or 565 fF (the sum of the feedback capacitors). The ratio of these gain (volts/x-ray) settings is 7.5:1. When in high gain the voltage change at the output of the CTIA is ~ 4.7 mV per 8-keV x-ray. In low gain, this value is ~ 0.62 mV per 8-keV x-ray.

Scattering from a non-crystalline sample falls off quickly as a function of scattering angle. The profile of the fall-off depends on the particle being studied, but is well defined and repeatable for a given particle. Because of this, the scattered intensity envelope for a particle can be measured and then a pixel-by-pixel 2-D programmable gain profile can be optimized for the data being collected. Pixels at small scattering angles are expected to be set in low-gain mode to maximize the full-well values. Pixels at larger scattering angles are expected to be set in high-gain mode to maximize the single-photon signal to noise ratio.

Before the signal from the front-end integrator is digitized, the voltage is sampled by the sample and hold stage (see Figure 1). The output of the sample and hold buffer is then digitized using single-slope digitization. The digitization scheme consists of a comparator with inputs of the in-pixel sampled voltage and a globally transmitted ramp signal[7]. A fourteen-bit, small-area ripple counter in each pixel is gated by the comparator, and counts clock pulses while the ramp signal falls. The binary number left in the counter after digitization is a measure of the output voltage sampled from the front-end charge integrator. This signal is proportional to the total absorbed x-ray energy. The time required for digitization is highly configurable and has been tested in prototypes with digitization times of less than 0.5 ms. The digitization time to be used in the final detector is approximately 2 ms. Readout of each 185x194 pixel chip happens in less than 6 ms through 8 digital output ports. The approximate bit-rate for each digital output port is 11 Mb/s.2.2 Silicon Detector Chip

The detector chip is a 500 micron thick high-resistivity (5-10 kΩ cm) silicon PiN diode. This high-resistivity material can be over-depleted using reverse bias voltages of less than 200 V. Measurements on previous PAD detectors indicate that the charge accumulation at room temperature due to dark current in the anticipated exposure time will be significantly less than that collected from the conversion of a single 8 keV x-ray[11]. The contribution of dark current to signal noise is therefore expected to be small when compared to other noise sources (discussed below). The quantum efficiency of the detector diode is expected to be >0.99. The diode is being fabricated by SINTEF (SINTEF Electronics and Cybernetics, Blinden, Oslo, Norway).

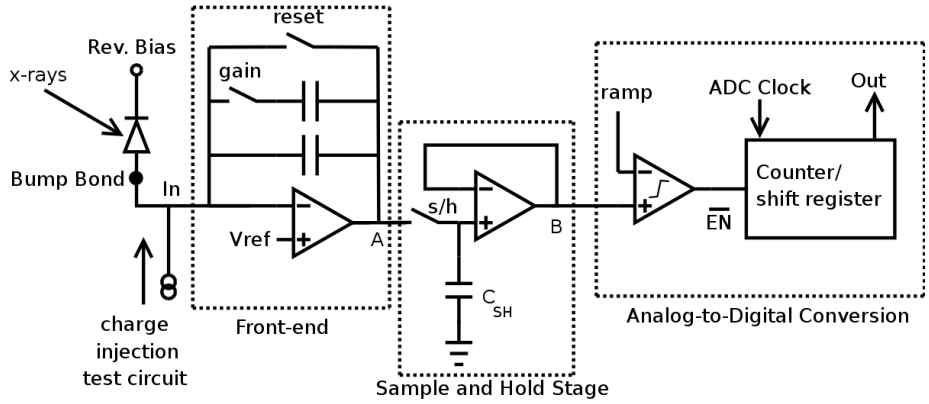

Figure 1: Simplified pixel schematic. The hybridized detector will have the bump-bonding connections between the detector diode and CMOS electronics at the node labeled "IN". All pixels have a switched capacitor charge injection circuit for testing pixel functionality and secondary verification of the calibrated gain profile.

3. PROTOTYPE TESTING

Three small-scale detector prototypes have been fabricated through the MOSIS service (Information Sciences Institute, University of Southern California, Marina Del Rey, CA USA) using the Taiwan Semiconductor Manufacturing Corporation (TSMC) 0.25 μm mixed-mode process. These prototypes were made to verify sub-circuit and small-scale array (16x16 pixels) functionality. Performance tests on the prototypes have concentrated on pixel functionality, noise performance, linearity and saturation levels. An in-pixel charge injection circuit, consisting of three transistors, was used to test pixel response in small-scale arrays.

3.1 Functionality

The prototypes have been used to verify and measure the performance of the front-end integrating stage, the one-bit programming of the front-end charge to voltage gain, the in-pixel analog-to-digital converter, the pixel addressing technique and the digital readout circuitry. Fig 2(a) shows the output of a single pixel in the low-gain configuration as a function of the number of charge injection operations.

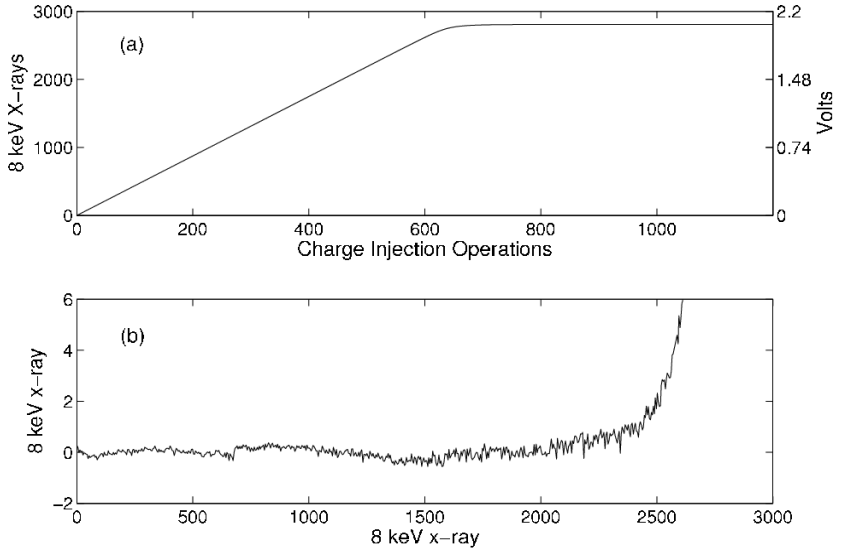

Figure 2: Top: The number of equivalent x-rays plotted against the number of charge injection operations for a pixel operating in the low-gain mode. The magnitude of the voltage deviation caused by the charge injection into the integrating stage is also shown on the right axis. Saturation is well above 2000 photons. Bottom: Residuals of a linear fit of a subset of the data.

3.2 Noise considerations

Low-illumination noise requirements can be satisfied by reducing the value of the front-end integration capacitance to increase the change in the output voltage (see node A in Figure 1) per x-ray detected. However, minimization of noise sources has the important benefit of reducing the required voltage per x-ray gain and allowing a larger full-well. Noise in the pixel (shown in Figure 1) was found to have three dominant source:

1. **Conversion noise:** Noise associated with in-pixel analog-to-digital conversion.

2. **Sampling noise:** Thermal noise from the front-end amplifier that is sampled onto the hold capacitor (C_{SH}) when opening the sample switch (labeled s/h in Figure 1).

3. **Reset noise:** Thermal noise sampled onto the input of the front-end integration stage (the node labeled "In" in Figure 1), when opening the reset switch.

The noise associated with the analog-to-digital conversion has been minimized by limiting the bandwidth of the comparator; carefully shielding and filtering the global ramp signal; and routing power to minimize coupling between analog and digital signals. Measurements on the prototypes indicate that the digitization noise is small compared to other noise sources listed. Switching time jitter of a lone comparator found a noise of 50 μV and tests of the pixel without latching the integrator or sample-and-hold circuit measured noise levels of 150 μV.

The noise associated with sampling the output of the front-end integration stage is proportional to the inverse square-root of the total capacitance used to sample the voltage. Since the integration stage does not require high bandwidth, the sampling capacitance has been made large, up to pixel area constraints, to reduce noise.

Reset noise is often a dominant noise source, especially when the pixel is configured in the high-gain mode. Following work in the CMOS imager community, the reset noise can be reduced by gradually transitioning the controlling gate voltage when opening the reset switch. This gradual transition reduces the bandwidth of the reset switch with respect to the front-end amplifier and limits its noise contribution[9]. For the high-gain pixel configuration the measured reset noise shows a reduction of 33% using a "soft-reset". This technique requires ≈50 μs for completion and is well suited for this detector since 50 μs is a small fraction of the time allotted for readout and the arrival time of the x-ray pulse is precisely known.

Pixel Size	110 μm x 110 μm
Frame Rate	120 Hz
Array Size	758 pixels x 758 pixels (84 mm x 84 mm)
RMS read noise	0.14 X-rays pixel (high-gain)
Full-well capacity	2 250 X-rays (low-gain)
Non-linearity (% full-well)	<0.5%
Detective Quantum Efficiency (DQE)	>0.9

Table 1: Measured, anticipated and calculated characteristics for the detector. Values given in terms of X-rays refer to 8 keV X-rays.

4. HIGH LEVEL ARRAY ARCHITECTURE

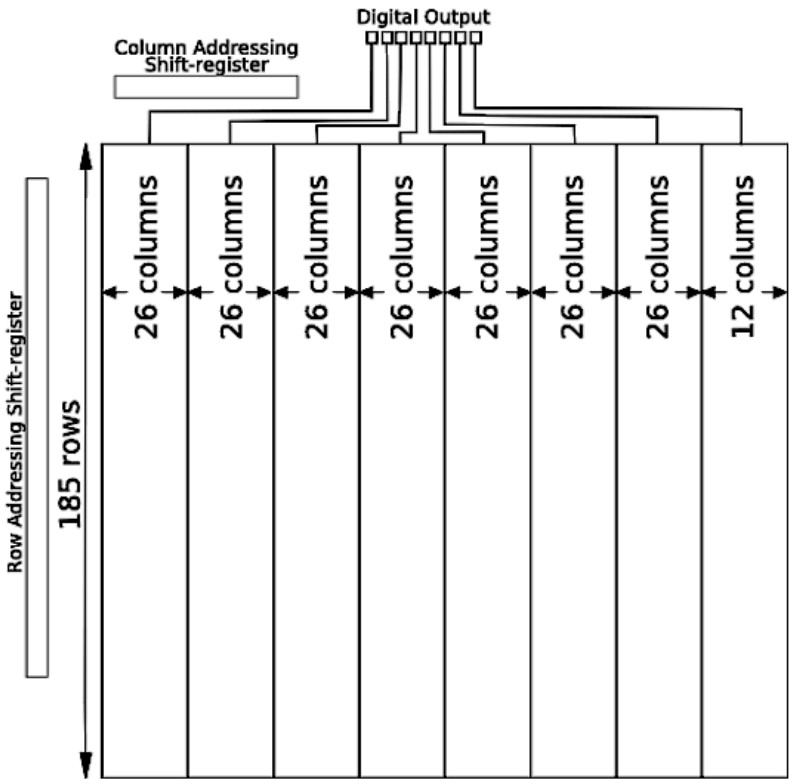

Figure 3: Diagram of the high-level readout chip architecture.

The full detector readout chip uses simple bit-passing shift-registers to address rows and columns. The pixels are divided into 8 banks (see Figure 3) and at any given time during the readout, one pixel in each of the eight banks is addressed. The digital output is eight bits wide allowing a pixel from each of the eight banks to be read simultaneously. Each bank consists of 26 columns of pixels except for one bank that has 12 columns. Adjacent columns of pixels are mirror images, helping to maintain a good separation between analog and digital signals.

5. DATA ACQUISITION AND CONTROL

The data acquisition (DAQ) and control system for the pixel array detector is designed in a hierarchical and modular manner using a Xilinx XC4V100FX FPGA based development board. Master/slave command handshaking across a PCI Express bus allows user control and monitoring in software. The DAQ and control system sets the detector mode of operation, provides low-level control of the image acquisition and read-out processes; and transfers the data to high-speed local storage. Low-level data processing such as re-ordering, frame formatting and lossless compression may also be required before data transfer. High-speed data recording is required for continuous image acquisition. At 120 Hz, a

full array will have an output data rate of 140 MB/s (noting that the 14-bits/pixel will be recorded in 16 bit words). A commercially available, off-the-shelf system capable of sustained data writing speeds of 200 MB/s to disk has been specified and will be used.

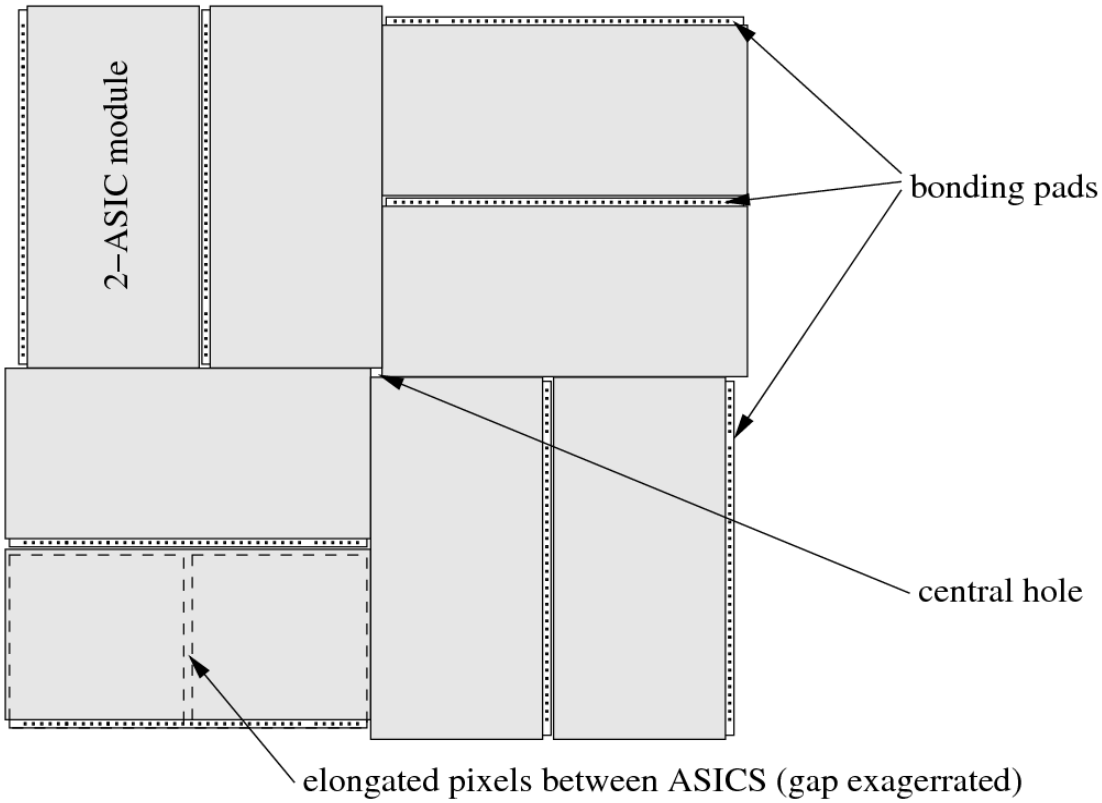

Figure 4: Top view of ASIC and module tiling for the LCLS PAD detector. The ASIC chips underneath the detector layer are indicated in the lower-left module by dashed-lines.

6. TILING AND CONSTRUCTION

The maximum CMOS readout chip is limited to an area of approximately 21 mm x 21 mm by the field of view of lithographic projection optics. Because of this, and the lack of readily available lithographic stitching for small volume research and development projects, tiling of multiple readout chips is necessary to develop a full, large-area detector. In contrast to the CMOS layer, the area of the detector diode array is only limited by the size of the wafer used for fabrication (in this case 150 mm diameter). This is because the minimum feature size required for diode fabrication is larger than that required for the CMOS readout chip and conventional 1:1 lithography is used. Tiling to make a large-area detector can be achieved by mating multiple readout chips to larger monolithic diodes arrays. Monolithic diode arrays mated to multiple readout chips have elongated diode pixels where the readout chips abut to allow for a gap between readout chips (see Figure 4).

The full detector will be a tiled array of modules. Each module consists of one monolithic detector chip mated to two CMOS ASICs. Only one edge of the CMOS chips has bonding pads, which allows gaps between modules to be minimized on the three edges without bonding pads, where the modules abut. The sides of the modules with wire-bonding pads will have a non-imaging area that is >1 mm wide. The edges of modules without bonding pads will have

a non-imaging width of approximately 500 μm. Phase retrieval applied to simulated scattering data indicates that the effects of the anticipated gaps between detector modules are not detrimental to structure determination.[10]

Because of the extreme intensity of the direct beam and the sensitivity of the experiment to parasitic scattering, a conventional beam-stop cannot be used and the detector will be designed with a central hole to allow the direct beam to pass unobstructed. Simulations show that the small-angle scattering profile contains information that is important for recovering molecular structure. The central hole must therefore be minimized so the detector pixels closest the central beam are able to capture this information.[10] The hole size specification for the final detector has not been determined, but there are a number of factors that limit how small the hole can be made. One consideration concerns diode guard rings that reduce leakage currents caused by the diode edge. The widths of these guard rings are roughly equivalent to the thickness of the diode (500 microns), and limit how close active pixels can be to the edge of the diode die.

Electrical connection between the detector diode and CMOS layers is made by bump-bonding. This is a non-trivial step that is required to make functioning detectors. We have contracted the services of RTI International (Research Triangle Park, NC) who specialize in flux-less solder bump-bonding using a plasma assisted oxide etch before hybridization. RTI electroplates solder into the openings of a thick photo-resist following the application of an under-bump-metalization. The process used for the LCLS PAD has been successful with other projects with pitches down to 50 microns and an interconnect density of 40:000 I/O cm.[11]

7. RADIATION DAMAGE

Work at CERN, Cornell and elsewhere has shown that smaller feature size CMOS processes, like the TSMC 0.25 micron process used for the LCLS PAD, and differential amplifier architectures are more resistant to radiation induced threshold shifts.[12,13] However, smaller CMOS feature sizes make designing analog storage elements more difficult because of increased transistor off-currents.

Radiation-induced charge accumulation within oxide can cause unwanted conduction between drain and source in nominally off NMOS devices. It can also cause leakage through the field oxide to nearby transistors. Using an enclosed layout for NMOS transistors ensures that current paths between the drain and source are regulated by the gate voltage and reduces radiation induced leakage.[14,15] The readout chip for the LCLS PAD uses enclosed NMOS transistors for critical switches in the analog signal path to increase radiation hardness.

8. FUTURE PLANS

The fabrication of full-sized readout and detector chips was begun in the winter of 2007. A functioning full-sized single-module prototype is planned for the Fall. The full detector chip is scheduled for delivery in 2008.

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