High-Speed X-ray Imaging with the Keck Pixel Array Detector (Keck PAD) for Time-Resolved Experiments at Synchrotron Sources

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Abstract. Modern storage rings are readily capable of providing intense x-ray pulses, tens of picoseconds in duration, millions of times per second. Exploiting the temporal structure of these x-ray sources opens avenues for studying rapid structural changes in materials. Many processes (e.g. crack propagation, deformation on impact, turbulence, etc.) differ in detail from one sample trial to the next and would benefit from the ability to record successive x-ray images with single x-ray sensitivity while framing at 5 to 10 MHz rates. To this end, we have pursued the development of fast x-ray imaging detectors capable of collecting bursts of images that enable the isolation of single synchrotron bunches and/or bunch trains. The detector technology used is the hybrid pixel array detector (PAD) with a charge integrating front-end, and high-speed, in-pixel signal storage elements. A 384×256 pixel version, the Keck-PAD, with 150 µm × 150 µm pixels and 8 dedicated in-pixel storage elements is operational, has been tested at CHESS, and has collected data for compression wave studies. An updated version with 27 dedicated storage capacitors and identical pixel size has been fabricated.

INTRODUCTION

Synchrotrons are pulsed x-ray sources because RF signals are used to accelerate charge carriers to relativistic speeds, yet few experiments conducted at synchrotrons take advantage of this pulsed nature to explore dynamic systems. This is largely because technology to take full advantage of the bunch structure of synchrotrons is not readily available. Images from isolated bunches may be obtained with fast shuttering systems, either electronic or physical, that are read out at a slow rate. However, imaging systems capable of matching the pulse arrival rate of, say, the Advanced Photon Source (APS) with a bunch arriving every 153 ns, present a rich set of technical problems. Photon counting pixel array detectors (PADs) are not typically usable because of their limited counting speed and, consequently, insufficient dynamic range for single pulse measurements when more than one photon is converted in a pixel. Integrating PADs, on the other hand can handle the signal with a larger dynamic range per pulse, but readout of the information is difficult to achieve because of issues with analog multiplexing across relatively large chips and, perhaps more importantly, data rates. A 128×128 pixel imaging array, with each pixel digitized to 12 bits, and being fully read out every 153 ns yields a staggering data rate of 1.29 Tbit/s. Handling data rates this high with present technology requires massively parallel readout, optical waveguide transmission [1, 2], fast data compression, and/or perhaps sparse event-driven readout. Fortunately, there is middle ground between collecting single images and continuous high-speed readout. Since in-pixel switching can be fast (less than nanoseconds), an array of sample-and-hold capacitors can be used as in-pixel analog storage. By synchronizing sample-and-hold cycles across all pixels, a PAD can effectively store images in distributed analog memory, saving the relatively slow process of reading out the chip for later.

This in-pixel analog storage technique is the approach taken by the Keck PAD and builds on previous work [3, 4]. The Keck PAD versions presented in this paper use full-scale detector chips with 128×128 pixels, and represents an enlarged version of previous 16×16 pixel prototypes [5, 6]. Similar in-pixel data storage techniques have also been incorporated into the Adaptive Gain Integrating Pixel Array Detector (AGIPD) [7].

TABLE 1. Keck PAD version 1 specifications.

Parameter	Value
Pixel Size	150 µm × 150 µm
Tile Size	128 × 128 pixels
Tiled Array	2 × 3 tiles
Sensor	500 µm thick Si
Noise (V)	860 µV (high gain)
Noise (x-ray equivalent)	0.7 8-keV x-ray (high gain)
Gain	1.8 ADU / 8-keV x-ray (high gain)
Full Well	1200 8-keV x-rays (high gain) 8000 8-keV x-rays (low gain)
Max. Frame Rate	~10 MHz
Read Time	< 1 ms/stored frame

DETECTOR DESIGN

Tiled Array

The Keck PAD detector, in its present form, is a 3×2 tiling of hybrid modules, similar mechanically and, to a large degree, electronically to the mixed-mode pixel array detector (MM-PAD) [8]. Each hybrid module has two layers: a custom designed CMOS integrated circuit (IC) fabricated with the TSMC 0.25 micron mixed-mode process and a high-resistivity silicon diode. The two layers are connected at the pixel level using lead-tin eutectic solder bump bonds to make a hybrid module with 128×128 imaging pixels. The full tiled array has 256×384 pixels. A list of specification are outlined in Table 1.

The tiled array is vacuum sealed and the sensor modules are regulated to −30°C using a thermo-electric cooler and chilled water (15°C). Each of the modules has 8 analog outputs that are digitized in close proximity to the chips. The detector control signals and data acquisition are controlled using a Xilinx Virtex 6 FPGA development board programmed with a flexible state-machine that allows for low-level custom control of the detector. Options for the state machine are passed to the FPGA by an ethernet connection and data is relayed from the FPGA to a data acquisition computer using the Camera Link Interface (full configuration). Hardware and software triggering are possible with this design. Hardware triggering is preferred for the low-latency, low-jitter performance necessary to take advantage of all the detector's high speed capabilities.

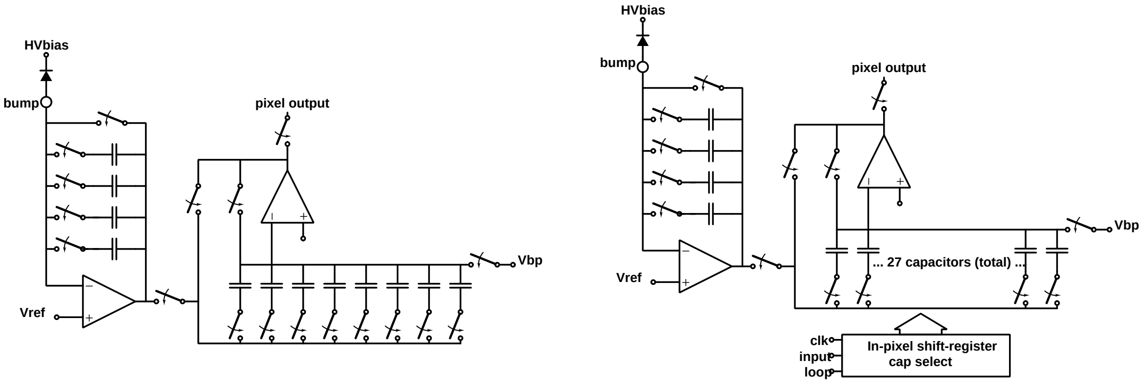
Pixel Design

The technical solution that provides high-speed framing to match the arrival frequency of single bunches is in-pixel analog storage. In-pixel storage eliminates the need for real-time transmission of voltages from pixels to off-chip analog-to-digital converters and enables fast "burst" framing that is limited in duration by the number of storage elements in the pixel.

In addition to in-pixel storage elements, the pixel design has other features that are either necessary or desirable in fast framing detectors. The first is a fast front-end amplifier that is capable of slewing charge on capacitors but maintains a relatively low quiescent current when charge is not being collected. This is achieved using a class AB amplifier design [9]. The second is four selectable feedback capacitors on the front-end that allow for the charge-to-voltage gain of the transimpedance integrating AB amplifier to be adjusted to levels appropriate for the data being collected. Beyond gain control, the feedback capacitors can be individually selected and cycled through without reset while acquiring data to allow for repeated sampling of cyclical processes before readout. In some situations, this improves the fidelity of the signal collected and provides an efficient avenue to collect charge without the relatively lengthy process of readout [9].

High-level, simplified pixel schematics for the Keck PAD versions are shown in Fig. 1. Version 1 has been fabricated, tested and used in experiments [10]. The version 2 CMOS has been fabricated and is being processed in preparation for hybridization. The main differences between the two designs are:

- An increase in the number of dedicated sampling capacitors from 8 to 27. This increases the number of frames that can be captured during each burst of framing.



Keck-PAD pixel version 1 Keck-PAD pixel version 2

FIGURE 1. High-level schematics of two version of the Keck PAD pixel. Version 1 has been fabricated, tested, and used in experiments. Version 2 is in post-processing for hybridization.

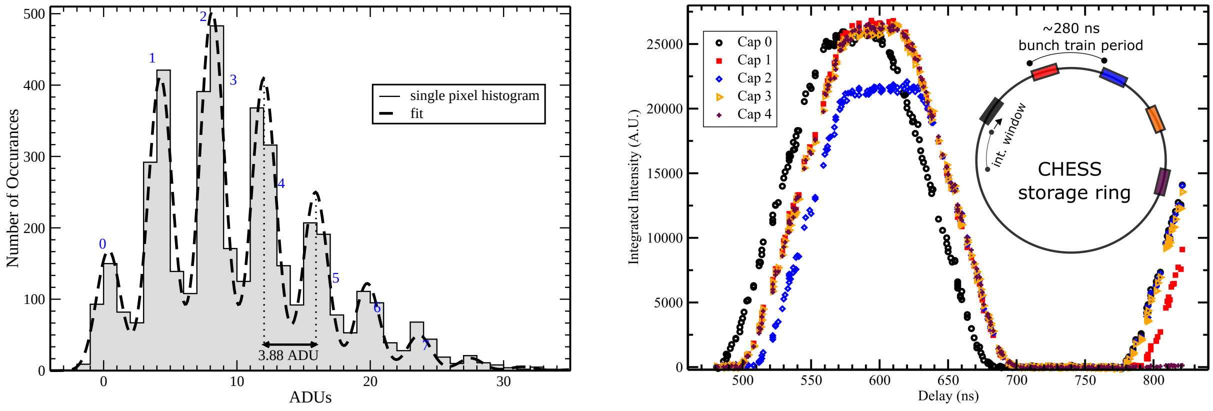
- A redesign of addressing logic for sampling capacitors to give maximum flexibility for operation while reducing the number of control lines routed across the array. Keck PAD version 1 has separate control lines for each capacitor that is suitable for small-scale prototypes, but cumbersome for full-chip routing. The increased number of storage capacitors in the Keck PAD version 2, precludes the sampling/storage capacitor control system used in Keck PAD version 1.
- A change in the gain levels that can be selected (via a feedback capacitor) to allow for improved sensitivity to lower energy x-rays. This is particularly important because high-speed experiments are often performed in the low-fluence regime, where single-photon thresholding can yield significant advantages [11].

PERFORMANCE

Keck PAD version 1 has been tested in the laboratory using a molybdenum anode x-ray source ($K_\alpha = 17.5\,keV$) and at Cornell High Energy Synchrotron Source (CHESS). Verification of the pixel's noise performance and signal gain is demonstrated with the response of a pixel to illumination with a zirconium-filtered molybdenum x-ray source through a 75 µm diameter pinhole in tungsten that is used to mask charge sharing regions of the pixel. Three-thousand repeated measurements were used to populate the histogram shown in Fig. 2a. Discrete peaks in the histogram correspond to integer numbers of photons. Though the analog-to-digital conversion under-samples the noise distribution of a single peak, fitting a Poisson distribution to the peak amplitudes and using a Gaussian model for the peaks gives a good indication of the noise (0.7 8-keV equivalent) and gain (1.8 ADU per 8-keV x-ray) of the detector. Note that signal scales with x-ray energy and that referencing 8-keV x-ray equivalent noise allows for a quick and direct comparison with other pixel array detectors [8, 11].

Dynamic performance was verified using the bunch structure of CHESS that comprises 5 groups of bunches ('bunch trains'). Each bunch train has 6 bunches and one of the bunch trains is less populated by charge carriers. By choosing an integration time of 140 ns with frame period matching the 280 ns bunch train period, and phasing the burst acquisition of frames with the Cornell Electron Storage Ring (CESR) synchronization signal, the profiles of the bunch train were mapped by summing the intensities of illuminated pixels. The results are shown in Fig. 2b. Important results include the ability to distinguish the less populated bunch train that was sampled by capacitor 2 and the ability to distinguish fine temporal detail of the arriving pulses that vary from the approximate bunch train period of 280 ns.

In addition to proof of concept tests and laboratory measurements of performance, the detector has been used to collect data for a study of magnesium alloys subjected to high-speed dynamic loading [10] at CHESS. Practical exercise of the detector to verify functionality, both in terms of data quality recorded by the detector and incorporation into a data acquisition environment, is invaluable for detector development.



(a) (b)

FIGURE 2. a) Keck PAD version 1 integer photon spectrum obtained by illuminating a pixel with a molybdenum x-ray tube source through 75 micron pinhole and histogramming the output of the pixel through 3000 frames. b)A demonstration of the temporal resolution obtained by Keck PAD version 1. The first five storage capacitors were used to capture bunch trains at CHESS using integration windows of 140 ns with a period of 280 ns and phased with the storage ring synchronization signal.

CONCLUSION

The Keck PAD, both versions 1 and 2, offers a practical solution for maximizing the scientific potential for dynamic studies at synchrotron source. The first version of the Keck PAD is scheduled for an experiment at the Advanced Photon Source in August 2015. The high-speed framing capabilities, moderate 150×150 micron pixel size, and monolithic tiling units of 128×128 pixels assembled into a 256×384 pixel array seems to offer many experimental opportunities. Interested collaborators should not hesitate to contact us.

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