High Dynamic Range X-ray Detector Pixel Architectures Utilizing Charge Removal

Joel T. Weiss, Katherine S. Shanks, Hugh T. Philipp, Julian Becker, Darol Chamberlain, Prafull Purohit, Mark W. Tate, Sol M. Gruner

Abstract—Several charge integrating CMOS pixel front-ends utilizing charge removal techniques have been fabricated to extend dynamic range for x-ray diffraction applications at synchrotron sources and x-ray free electron lasers (XFELs). The pixels described herein build on the Mixed Mode Pixel Array Detector (MM-PAD) framework, developed previously by our group to perform high dynamic range imaging. These new pixels boast several orders of magnitude improvement in maximum flux over the MM-PAD, which is capable of measuring a sustained flux in excess of 10^8 x-rays/pixel/second while maintaining sensitivity to smaller signals, down to single x-rays. To extend dynamic range, charge is removed from the integration node of the front-end amplifier without interrupting integration. The number of times this process occurs is recorded by a digital counter in the pixel. The parameter limiting full well is thereby shifted from the size of an integration capacitor to the depth of a digital counter. The result is similar to that achieved by counting pixel array detectors, but the integrators presented here are designed to tolerate a sustained flux $>10^{11}$ x-rays/pixel/second. Pixel front-end linearity was evaluated by direct current injection and results are presented. A small-scale readout ASIC utilizing these pixel architectures has been fabricated and the use of these architectures to increase single x-ray pulse dynamic range at XFELs is discussed briefly.

I. INTRODUCTION

ADVANCES in synchrotron radiation light source technology have opened new lines of inquiry in material science, biology, and everything in between. However, x-ray detector capabilities must advance in concert with light source technology to fully realize experimental possibilities. X-ray free electron lasers (XFELs) place particularly large demands on the capabilities of detectors, and developments towards diffraction-limited storage ring sources also necessitate detectors capable of measuring very high flux [1], [2], [3].

For example, in coherent diffractive imaging experiments, measurement of both the intense direct beam and very low fluence wide angle scatter at the same time greatly facilitates sample reconstruction [4]. This necessitates a detector capable of measuring not only high sustained flux, but also very small signals simultaneously.

Detectors with wide dynamic ranges are needed to bridge the gap between x-ray light source technology and detector technology. Previously, our group collaboratively designed a Mixed Mode Pixel Array Detector (MM-PAD) to operate

J. T. Weiss, J. Becker, D. Chamerlain, and S. M. Gruner are with the Cornell High Energy Synchrotron Source (CHESS) and the Cornell Laboratory of Atomic and Solid State Physics.

K. S. Shanks, H. T. Philipp, P. Purohit, and M. W. Tate are with the Cornell Laboratory of Atomic and Solid State Physics.

along these lines [5], [6]. MM-PAD functionality will be discussed briefly. The present work describes an ASIC containing several pixel front-end test structures which build on the MM-PAD detector framework. Measurements from these test structures are presented.

II. DYNAMIC RANGE EXTENSION BY CHARGE REMOVAL

The full well of a simple integrating pixel, defined as the amount of integrated photocurrent that can be stored in such a pixel, is limited by the size of the front-end amplifier feedback capacitance for a given output voltage swing. Increasing the integration capacitance to increase full well is ultimately constrained by pixel size. Perhaps more importantly however, a larger integration capacitance couples the output noise of the integrating amplifier to its front-end more strongly, leading to a larger equivalent noise charge, and thereby obscuring small signals. Thus increasing the well depth of an integrating pixel while maintaining sensitivity to single photon signals requires architectures more sophisticated than a simple, traditional integrator.

Dynamic range extension of an integrating pixel can be achieved in many ways, one of which is eliminating integrated charge to prevent integrator saturation. If this is done in a controlled way, the total integrated charge can be reconstructed. For example, the readout ASICs described in [7] and [8] each use charge pumps to systematically eliminate integrated charge, and the number of charge pumps utilized is recorded as a digital conversion. The MM-PAD performs this digitization in each pixel of a two dimensional array.

In the MM-PAD, photocurrent resulting from absorption of x-rays in a reverse-biased photodiode is integrated onto a charge sensitive amplifier whose output is monitored by a comparator. When the amplifier output (V_{out} in figure 1) crosses an externally set threshold (V_{th} in figure 1), a gated oscillator is enabled that triggers a counter and the switched capacitor circuit enclosed in the dotted box in figure 1. With each pulse of the gated oscillator this switched capacitor removes a fixed quantity of charge ($\Delta Q = C_{rem}(V_{front-end} - V_{low})$) from the integration node while an in-pixel counter is incremented. The charge removal incurs no dead time and helps the integrator avoid saturation. The integration capacitance is sized such that the signal from a single 8 keV x-ray is readily measurable with excellent signal to noise. This strategy shifts the full well limiting parameter from the size of a capacitor to the depth of the in-pixel digital counter.

The MM-PAD achieves a full well of 4×10^7 8 keV x-rays/pixel/frame in addition to framing at 1kHz [5]. The pixel
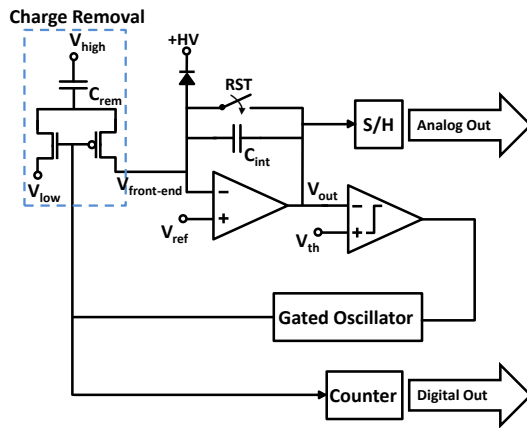
Fig. 1. Simplified MM-PAD schematic. The switched capacitor for charge removal is enclosed in the dotted box. In figures 1 to 4 the input results from x-rays stopped in the reverse-biased diode attached to +HV.

array is composed of six modules butted in a 2x3 array, and each module is composed of 128x128 pixels with 150μm pitch.

Mixing digital and analog modes in the MM-PAD has limitations. Most prominently, in the existing design, digitization and removal of integrated charge is limited to a rate of 2MHz. This is the maximum speed at which the in-pixel gated oscillator was designed to run. Reliable charge integration in the high flux regime requires that, once the charge removal capacitor is connected to the integration node, the node returns to virtual ground before it is disconnected. Deviation from this behavior leads to uncertainty in ΔQ, the charge removed per oscillator cycle. The MM-PAD amplifier meets this requirement within its design specifications, but the question of front-end virtual ground fidelity becomes more challenging with larger inputs, particularly for high peak photocurrent. In the MM-PAD, the charge removed per gated oscillator cycle is roughly equal to the integrated photocurrent generated by 200 8 keV x-rays converted in the silicon x-ray sensor, resulting in a sustained flux capability of 4×10^8 8 keV x-rays/pixel/s.

The goal of the present work is to create pixels which tolerate an even greater sustained flux than the MM-PAD. Within the MM-PAD framework, this requires increasing the maximum rate of charge removal events and increasing the charge removed in each cycle. Three new pixel designs that accomplish this are summarized below.

III. NEW CHARGE REMOVAL STRATEGIES

Three high dynamic range pixel architectures relying on charge removal techniques were developed [9]. The front-ends of these pixels were laid out and fabricated in TSMC 180nm mixed-signal CMOS. This process was chosen for its 2fF/μm² MIM capacitors, thick top metal, and balance of transistor speed, supply voltage headroom, and cost. Each pixel variant described in this work is designed for pixel arrays with 150μm pitch.

A. MM-PAD 2.0

The first pixel architecture is a scaled version of the original MM-PAD and is depicted in figure 2. In contrast to the MM-

PAD, the MM-PAD 2.0 incorporates adaptive gain, as demonstrated previously by detectors such as the AGIPD [10]. The MM-PAD 2.0's charge removal circuit will not trigger unless the lowest-gain stage has already been engaged. This allows the use of a larger charge removal capacitor than in the original MM-PAD, thereby increasing ΔQ. In the readout ASIC discussed here, 6 combinations of total feedback capacitance and charge removal capacitance were tested. Charge removal capacitors ranged from 440fF to 2630fF with equal or greater total feedback capacitors in each case. Larger charge removal capacitors allow a pixel to integrate higher photocurrents by increasing ΔQ. However, charge removal capacitors of 1800fF and 2630fF (with matched feedback capacitors) exhibited incomplete charge removal at the maximum oscillator frequency. Based on simulations, this is most likely due to the RC constant of the charge removal circuit, which increases with the size of the charge removal capacitor. A version of the pixel with a total maximum feedback capacitance of 2630fF and a charge removal capacitance of 880fF exhibited the most robust performance. The results presented in section V are from this variant. The high-gain stage has a feedback capacitance of 40fF, small enough to resolve the signal from one 8 keV x-ray. To increase measurable sustained flux further, the maximum frequency of charge removal has been increased by a factor of 50.

Integrating high flux signals requires commensurate amplifier slew rates. The integrating amplifier of the MM-PAD 2.0 is a class AB operational transconductance amplifier based on [11]. This topology was chosen for its high current output, boosted by local common-mode feedback, rapid settling time, and relatively low power consumption. The comparator employed is asynchronous and optimized for response time. It is composed of a five transistor differential amplifier driving an inverter.

As in the original MM-PAD, the charge removal circuitry consists of a gated oscillator which toggles a switched capacitor (not explicitly shown in figure 2) to remove charge from the integration node. The gated oscillator pulse width and maximum frequency is set by a capacitor and a tunable current mirror. The MM-PAD 2.0 can tolerate larger photocurrent spikes (integrating $> 10^3$ x-rays before relying on charge removal) and larger sustained photocurrents than the original MM-PAD.

B. Charge Dump Oscillator (CDO)

The CDO pixel design aims to scale the rate of charge removal with the rate of charge arrival by combining the charge removal switched capacitor with the oscillator driving it. Depicted in figure 3, the frequency of charge removal is set by the propagation of digital signals in the ring oscillator and the charging rate of the removal capacitor, C_{rem}. When a comparator indicates that a threshold has been crossed, the oscillator is activated and C_{rem} connects to the integration node. Once C_{rem} has charged to the switching threshold of the adjacent inverter, the capacitor is detached and the charge accumulated onto it is dumped to ground. The faster C_{rem} charges while attached to the front-end, the faster charge is removed.
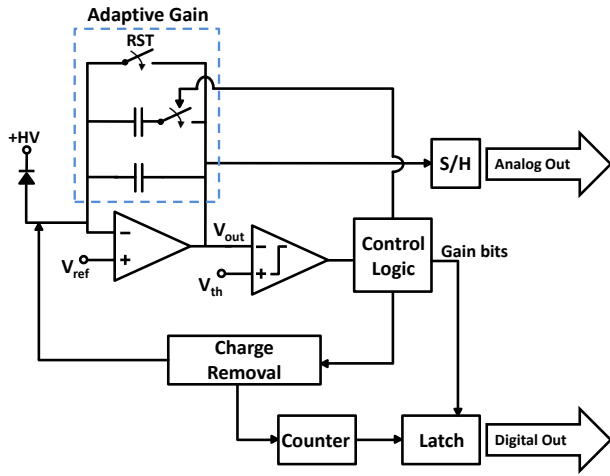
Fig. 2. Simplified MM-PAD 2.0 schematic. Control logic box engages adaptive gain (enclosed in the dotted box) prior to enabling switched capacitor charge removal.
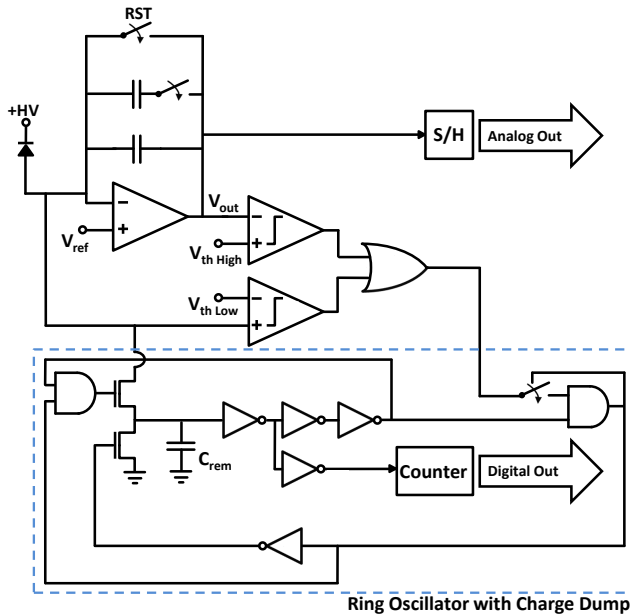

Fig. 3. Simplified CDO schematic. The ring oscillator charge removal circuitry is enclosed in the dotted box. Selectable gain was replaced with an adaptive gain scheme in the most recent fabrication.
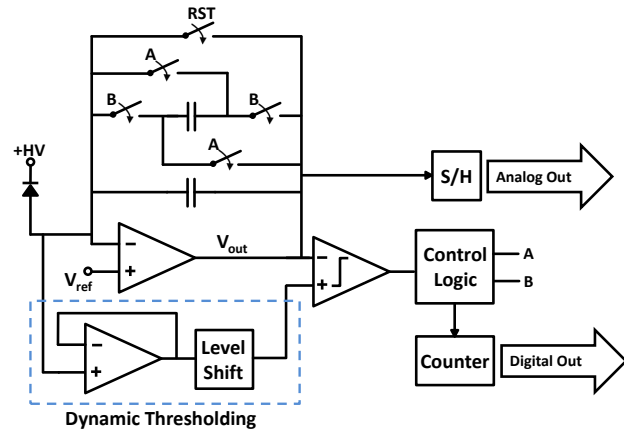

Fig. 4. Simplified capacitor flipping pixel schematic. Dynamic thresholding circuitry is enclosed in the dotted box. An adaptive gain scheme was implemented in the most recent fabrication.

In addition to one comparator monitoring the integrator output, as in the MM-PAD, a second comparator monitors the pixel front-end voltage. Charge removal is also triggered by any significant deviations of this voltage from V_{ref}. Deviations from V_{ref} indicate that the integrator is unable to keep up with incident photocurrent, in which case charge removal is needed. If the integration node is unable to be maintained at V_{ref} some error in integration is inevitable.

At low x-ray flux, the circuit operates similarly to the MM-PAD, but the tracking of charge removal rate with incident photocurrent should allow the CDO to continuously integrate larger sustained inputs. While the inverter thresholding of the CDO is very fast, it is more susceptible to fabrication process variation than the other designs presented here. In this case,

variation could result in different quantities of charge removed per cycle in each pixel. Although this can be calibrated, it is an additional complication. As depicted in figure 3 the CDO variation tested here utilizes a selectable gain, which was replaced with adaptive gain circuitry in the 16x16 pixel array test ASIC described in section VII. Additionally, the integrating amplifier studied here is a simple, five transistor differential amplifier. The amplifier is intentionally incapable of high current integration. Its use was intended to ensure that the pixel in this test ASIC would rely on the charge dump oscillator circuitry. The amplifier has been replaced by a class AB amplifier similar to that of the MM-PAD 2.0 in subsequent pixel iterations. Both comparators in the pixel are asynchronous.

C. Capacitor Flipping Charge Removal

The third pixel front-end fabricated and tested relies on a charge removal method based on the flipped capacitor filter described in [12]. The capacitor flipping pixel integrator uses two equally sized integration capacitors connected in parallel, depicted in figure 4. One of the two integration capacitors is connected via a network of CMOS switches so as to allow the capacitor's polarity in the circuit to be reversed. Adaptive gain was not incorporated in the initial fabrication and is not shown in figure 4, but it was implemented in the 16x16 pixel array test ASIC described in section VII.

Referring to figure 4, the pixel begins integration with the switches labeled A closed and the switches labeled B open. Charge is integrated onto both equal-sized capacitors in parallel. When the integrator's output crosses the comparator threshold, the comparator fires. This activates the control logic which opens switches A. After a brief delay to prevent shorting the integration capacitors, switches B are closed. This reverses the orientation of half of the integration capacitance. As a result, integrated positive charge on each capacitor neutralizes negative charge on the other capacitor. Thus, the integrator is effectively reset, and can continue integrating photocurrent. Subsequent flipping occurs as needed. Connections to the

flipping capacitor are always broken before new connections are made.

As with each other charge removal circuit, ΔQ depends on the front-end voltage of the integrator. To reduce the error introduced by changes in the front-end voltage due to large current spikes, a dynamic thresholding circuit was devised. In its present implementation, the pixel comparator can use an external reference voltage to define the threshold at which capacitor flipping is initiated, or it can be set dynamically. In the dynamic case, a level-shifted copy of the front-end voltage is used to set the capacitor flipping threshold voltage. This ensures that there is a specific voltage across the integration capacitance at the time of the comparator firing, precisely the level shift voltage. However, due to the dependance of ΔQ in this method on both in the integrator input and output nodes, an input rate dependent error is introduced by delays in the capacitor flipping control logic. These errors are investigated in section V.

The dynamic thresholding block level schematic is depicted in figure 4. The level shift is set by a diode drop within the pixel. The integrating amplifier of the capacitor flipping pixel is a class AB amplifier similar to that of the MM-PAD 2.0, but optimized to interact with this alternative charge removal method. The comparator is again asynchronous: a five transistor differential amplifier driving two inverters. The gated oscillator which controls the capacitor flipping is a ring oscillator.

IV. CONSTANT CURRENT INTEGRATION

The three pixel front-ends were fabricated with several means of injecting a test charge to emulate an input x-ray signal. A PMOS current source in each pixel provided simple functionality tests. For higher currents and quantitative results, a copy of each pixel with a probe pad attached to its input was included in fabrication. Current was injected into pixels through a tungsten needle with a $10\text{k}\Omega$ resistor between the needle and an external current source. The current was generated and regulated by a Keithley 2400 Sourcemeter. Output signals were buffered off chip to a DPO7254C Tektronix oscilloscope.

Parasitic capacitance of the needle probe was estimated to be $\sim$10pF. This estimate is based on the change of V_{out} in the MM-PAD 2.0 pixel during a charge removal event. The integrating amplifier output voltage jumps during charge removal to maintain V_{ref} on the front-end. The jump is smaller with the needle contacting the front-end because the needle's parasitic capacitance reduces the charge transfer efficiency of the integrating amplifier, i.e. charge removal pulls some charge from the parasitic capacitance rather than the integration capacitance. This parasitic capacitance is significantly larger than the contribution expected from a bump bonded sensor, which is closer to 200fF. Based on calculations of charge transfer efficiency and simulation results, this increased parasitic capacitance reduces the maximum signals which can be properly integrated as a result of reducing ΔQ. The capacitance also has a damping effect on pixel front-end transient signals. Consequently this method is not suitable for

testing pixel performance under pulsed input, but these results do indicate the magnitude of average input signal rates which can be integrated by the pixels under investigation.

V. RESULTS

A. Linearity of Integration

To evaluate the linearity of integration for each pixel architecture, pixel output was monitored with a constant current input. The measured output, charge removal frequency, was multiplied by nominal ΔQ values (the quantity of charge removed per removal execution) to calculate an inferred input current. This inferred input current can then be compared to the actual, known input current. These values are plotted against each other in figure 5. To measure the charge removal frequency, buffered charge removal control signals were measured on an oscilloscope, and edge finding algorithms were used to determine the time of each charge removal cycle. Linear fits to the time of each charge removal versus the number of charge removals preceding it yielded the charge removal period as the slope of the fit. From this, frequency and uncertainty in the determination of the frequency were extracted. Variations in frequency between traces at a given input current were larger than the uncertainty in the determination of the frequency in a single trace, but both measures of uncertainty are smaller than the data points plotted in figure 5. Voltages used in the calculation of charge removal quantities were taken at their nominal values, e.g., $V_{\text{front-end}}$ was taken as V_{ref}, which is set externally. Throughout this section, current is specified in units of equivalent 8 keV x-rays/s. This is the flux of 8 keV x-rays that, when absorbed in a reverse biased silicon diode, would produce an equivalent photocurrent.

The MM-PAD 2.0 results are shown as triangles in figure 5. Good performance is seen with inputs up to $1.3\text{x}10^{11}$ 8 keV x-rays/s equivalent. The inferred current measurement abruptly plateaus, indicating that the pixel oscillator is operating at its maximum frequency. These values are consistent with simulation. Deviation from linearity is likely a result of process variation in charge removal capacitor size and $V_{\text{front-end}}$ not being held precisely at V_{ref}. This can be calibrated.

The CDO results are shown as circles in figure 5. At low input currents, the inferred input is greater than the actual input, which implies that ΔQ is less than what is expected based on the value of V_{ref}. This could be a result of process variation in capacitor size. Alternatively, incomplete charge removal may occur because signals in the ring oscillator propagate quickly compared to time constants associated with the charge dump process. If the dump is repeatable, the digital gain of each pixel can be calibrated. However, because the switching of the CDO is regulated by the threshold of an inverter, the stability of any calibration is threatened over time by radiation damage which can result in device threshold shifts.

As the input current increases, the CDO's inferred input current drops below the actual input current. In this regime, above 10^{11} x-rays/s, the quantity of charge removed per charge removal execution exceeds the expected value. A likely cause of this error is a significant rise in the pixel front-end
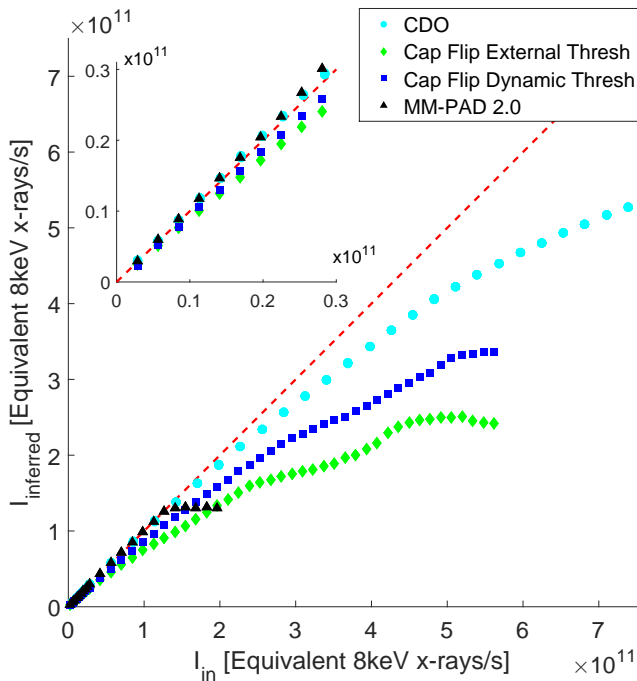
Fig. 5. Inferred input currents based on pixel outputs versus actual input current. The dotted line represents an ideal response (inferred input equals actual input). The charge dump oscillator is plotted with circles, the MM-PAD 2.0 with triangles, the externally thesholded capacitor flipping pixel with diamonds, and the dynamically thesholded capacitor flipping pixel with squares. Input and inferred current values are converted to the number of 8 keV x-rays absorbed in silicon per second which would produce an equivalent photocurrent. Inset: Magnification of the same data.

voltage above V_{ref}. This would cause more integrated charge to be removed from the integration node than intended.

Capacitor flipping pixel data was taken with both dynamic thresholding and a fixed, external threshold. These data are plotted in figure 5 as squares and diamonds, respectively. Some error in externally thresholded operation is a result of the integrator front-end voltage drifting upwards with higher input currents. This drift was observed directly in testing. The decrease of inferred current above 5×10^{11} 8 keV x-rays/s equivalent input in the externally thresholded case is likely a result of the front-end voltage being pushed outside of the integrating amplifier's range of optimal operating conditions.

A clear improvement in performance is seen with the dynamic thresholding enabled. However, there is still substantial error in the input reconstruction: less than 70% of the input is accounted for above 3.5×10^{11} x-rays/s equivalent input. This error can be explained by noting that the quantity of charge neutralized per capacitor flip, ΔQ, depends on the voltage across the integrator, not just the front-end voltage as in the other pixel designs. This means that any delay between when the capacitor should be disconnected and when it actually does disconnect can introduce error. Specifically, if photocurrent continues to be integrated during this delay, the output voltage of the integrator will continue to drop and the charge neutralized will be greater than anticipated.

From these data we can extract the error per capacitor flip. This is the difference between actual and inferred input
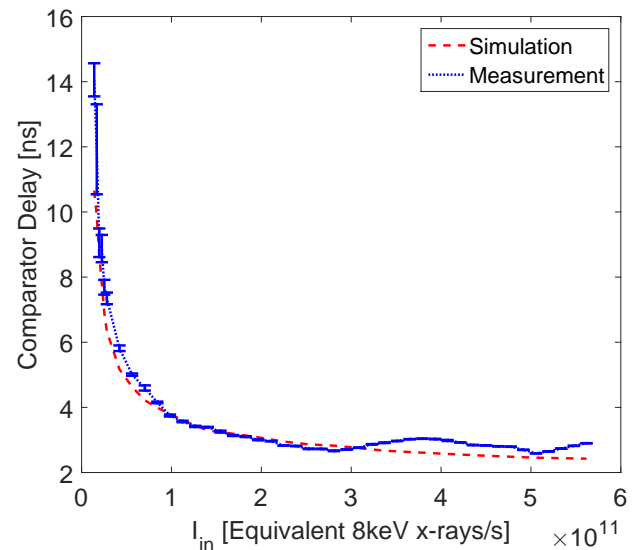

Fig. 6. Measured comparator delays from the capacitor flipping pixel with dynamic thresholding are plotted. Measured values assume that all deviations from linearity in the capacitor flipping pixel's output are a result of charge integrated during switching delays. Values from simulation are plotted as a dotted line.

currents divided by the frequency of capacitor flipping. Put another way, this is the charge removed per capacitor flip beyond what is expected based on the value of the level shift. Simulations of the comparator employed in this particular pixel front-end show that its firing delay varies with input falling edge slope, or equivalently in this case, input current. If we assume that all of this deviation from linearity is a result of photocurrent accumulation during the switching delay, dividing the error per capacitor flip by input current yields a measurement of this delay. Figure 6 plots the measured delays (assuming that all error comes from the delay) on top of the switching delays from simulation, both as functions of input current.

The measurement appears to follow the simulated values. This highlights a problem inherent to the capacitor flipping charge removal design. Any delay between when the capacitor should flip and when it actually does creates a window in which integrated charge will not be accounted for. Some of the calculated error may be due to an offset in the comparator threshold, but potential for input rate dependent error is ultimately inherent to the design.

B. Power Consumption

While maximizing the input range of pixels, it is essential to keep power consumption manageable. Power consumption was measured in simulation for each pixel substructure and is listed in Table I. Performance of the pixels in simulation was commensurate with their measured performance. These power consumption figures have been deemed suitable for scaling to full arrays with a planned 150μm pixel pitch in a 128x128 pixel array. Based on experience with previous detectors such as the MM-PAD, the temperature of a single ASIC can be sufficiently regulated by a water cooled peltier module providing 3-5W cooling power.

TABLE I
PIXEL AVERAGE POWER CONSUMPTION FROM SIMULATION

		MM-PAD 2.0	CDO	Cap Flip
Active Power (Integrating 10^{11} 8 keV x-rays/s)	Analog	146μW	52.7μW	158μW
	Digital	79.8μW	130μW	27.2μW
	Total	**226μW**	**183μW**	**185μW**
Quiescent Power	Analog	102μW	52.7μW	194μW
	Digital	3.63nW	775nW	0.563nW
	Total	**102μW**	**53.5μW**	**194μW**

The capacitor flipping pixel exhibits decreased analog power consumption under high loads. This is because the integrating amplifier in this pixel is a class AB amplifier, and after triggering a charge removal event, it is not required to slew back up to achieve its quiescent voltage. Instead, integrated charge is transferred to the integrator output by the capacitor flipping, and voltage is restored with minimal current supplied by the amplifier. This is not the case in the other pixel architectures.

VI. POTENTIAL APPLICATION TO XFELS

Charge removal circuitry is a valuable tool to extend measurable signal levels when a large, sustained photocurrent is generated in a pixel. XFELs produce exceedingly bright x-ray pulses with durations on the order of femtoseconds. It would seem that charge removal is ill-suited to the problem of integrating large XFEL pulses because no circuitry can respond on femtosecond time scales.

However, the peak photocurrent generated in pixels by XFEL pulses is not quite as dire as femtosecond x-ray pulse durations suggest. While an entire XFEL pulse reaches a detector in the span of femtoseconds, drift, diffusion, and the plasma effect cause the resulting photocurrent to take significantly longer to arrive at pixel integration nodes [13].

The plasma effect refers to the case when a sufficiently large number of electron-hole pairs are generated in a sufficiently small volume of the photo-sensor so as to behave like a plasma cloud. X-ray pulses of sufficient intensity can lead to the plasma effect in silicon diodes. The electron-hole plasma expels the photodiode electric field which would ordinarily separate charge carriers and bring them to respective sensor terminals. Instead, the surface of the plasma cloud is wicked away by the expelled electric field while the interior of the plasma remains relatively shielded. This slows down the accumulation of photocurrent at the pixel integration nodes.

To better understand this process, and to assess the prospect of operation at XFELs, we have utilized the transient current technique to measure photocurrent transients from a pixelated silicon diode illuminated by a focused infrared laser, as described in [14]. Laser wavelengths were chosen to match the attenuation length of x-ray photons in silicon. For example, 950 nm infrared light has the same attenuation length in silicon at room temperature as 8 keV x-rays. As a result, absorption of an intense 950 nm laser pulse in a silicon diode produces an electron-hole pair distribution in the sensor which is similar to what we might expect from a pulse of 8 keV x-rays.
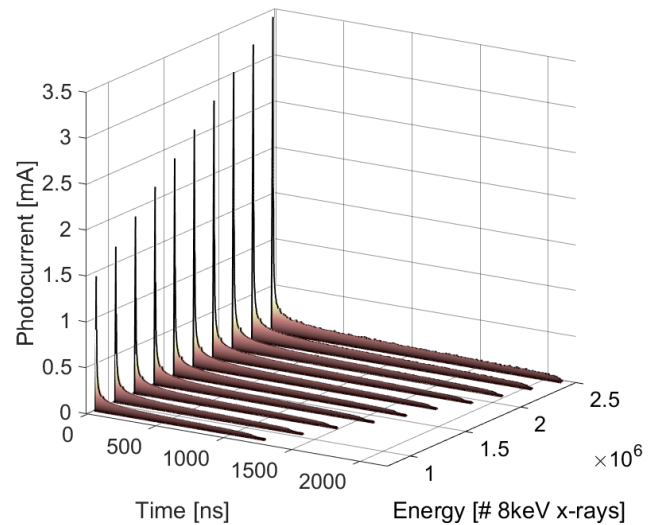

Fig. 7. Averaged photocurrent traces from 950nm picosecond laser pulses focused to 6μm incident on a 500μm thick silicon diode biased at 200V. Measurements were taken with the apparatus described in [14].

Figure 7 is a plot of averaged photocurrent transients collected from a silicon diode similar to the diode used in the MM-PAD. Generally speaking, photocurrent arrives in two phases: an initial spike arising largely from induced current [15] followed by a long tail as charge carriers drift to the sensor terminals. In the transients plotted, roughly 10% of total deposited charge arrives in the spike followed by a tail photocurrent on the order of 10^{11} equivalent 8keV x-rays/s. However, these numbers vary significantly based on factors including photon energy, area illuminated, and sensor bias, among others, as outlined in [14]. A strategy to integrate pulses of this nature might involve adaptive gain handling integration of the initial photocurrent spike and charge removal circuitry handling the drawn out tail. A small scale detector prototype featuring the pixels described above, with a bump bonded silicon photodiode, will be used to image these laser pulses and assess the viability of this strategy.

VII. SUMMARY AND FUTURE WORK

The performance of the pixel substructures discussed above demonstrates that each is capable of integrating large quantities of photocurrent. The MM-PAD 2.0 exhibits robust performance up to the design goal of 10^{11} 8 keV x-rays/pixel/s and has demonstrated the viability of adaptive gain in conjunction with charge removal.

The CDO appears to handle very high input currents better than the other pixel prototypes, but the CDO also presents a number of development risks. Since the CDO pixel relies on the threshold voltage of a digital inverter to regulate the removal of charge, pixel-to-pixel variation and calibration stability are potential weaknesses of the design. As a practical matter, small, static pixel-to-pixel variations in charge removal amounts can be accounted for with detector calibration. A greater concern is calibration stability because radiation exposure can induce threshold shifts. As a general scheme, the CDO does offer a possible avenue for the development

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2017.2679540, IEEE Transactions on Nuclear Science

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of high-speed charge removal and in-pixel analog-to-digital conversion, but the trade-offs are not well known and the degree of pixel to pixel variations in the CDO have not yet been studied.

The capacitor flipping pixel exhibits a systematic deviation from linearity which is ultimately undesirable in an x-ray pixel for scientific work, but the effectiveness of the dynamic thresholding concept is demonstrated. This dynamic adjustment for deviations of the pixel front-end voltage from V_{ref} could be utilized in other ways. For example, in the MM-PAD ΔQ is set by the difference between $V_{front-end}$ and V_{low}. V_{low} could be dynamically adjusted relative to $V_{front-end}$. In this way, a constant ΔQ can be enforced in the face of changing front-end voltages.

The pixel front-ends discussed above have been developed into full pixels and fabricated as a test ASIC. The ASIC has a 16x16 pixel array with four different pixel designs (the MM-PAD 2.0, the CDO, the flipping capacitor, and a modification of the MM-PAD 2.0 with dynamically adjusted V_{low}), each with an in-pixel counter, adaptive gain, fully functional readout, and addressable, in-pixel input current sources for functional testing.

The array will be bump bonded to a 16x16 pixel silicon sensor to test pixel performance with the integration of x-rays and infrared laser pulses. An additional row of pixels have been fabricated with probe pad inputs to allow direct current injection testing as described in this paper. The pixel array will be used to test integration performance at both high and low fluence. Testing of this pixel array detector will begin in late 2016.

ACKNOWLEDGMENTS

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